INTERNATIONAL WORKSHOP ON DEVICE TECHNOLOGY:

Alternatives to SiO_2 as Gate Dielectric for Future Si-Based Microelectronics

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MRS

Materials Research Society – Workshop Series

Based on "O Gaucho", by Nelson Jungbluth

Research and Development Pole in Microelectronics and Informatics Technology – CEITEC

Hotel Embaixador, Porto Alegre, Brazil
September 3-5 2001

Final Program

Sunday September, 2nd		Monday September, 3rd	Tuesday September, 4th	Wednesday September, 5th
		Chairperson Rita M. C. Almeida	Chairperson Jonder Morais	Chairperson Takeo Hattori
	8:30	Eric Garfunkel Rutgers University	Ravi Droopad Motorola	Douglas Buchanan IBM
	9:00	Glenn Wilk Agere Systems	Hiroshi Iwai Tokyo Institute of Technology	Luigi Colombo Texas Instruments
	9:30	COFFEE BREAK	Michel Houssa IMEC	Chris Werkhoven ASM America
	0:00	Elisa B.O. da Rosa UFRGS	COFFEE BREAK	
	10:30	Henry A. Kurtz University of Memphis	Dolf Landheer NRC Canada	Martin Green Agere Systems
	11:00	Gerald Lucovsky NCSU	Seichi Miyazaki Hiroshima University	Gregory Parsons NCSU
	11:30	LUNCH	Veena Misra NCSU	Laurent Gosset CEA-Grenoble
		LUNCH		
		Chairperson Dolf Landheer	Chairperson Veena Misra	Chairperson Fernanda C. Stedile
	14:00	Cristiano Krug UFRGS	Leonard Feldman Vanderbilt University	Kyeongjae Cho Stanford University
	14:30	Hsing-Huang Tseng Motorola	Cláudio Radtke UFRGS	Antonio J.R. da Silva São Paulo University
18:00 OPENING Renato de Oliveira State Secretary for Science and Technology Martin Green President – MRS Wrana Panizzi President - UFRGS	15:00	Jurgen von Bardeleben Paris University	Patrick Soukiassian CEA-Saclay	Alfredo Pasquarello IRRMA
		COFFEE BREAK		
	16:00	Takeo Hattori Musashi Institute of Technology	POSTER SESSION (5 min ORAL PRESENTATION)*	Panel Review and Final Discussion
	16:30	Evgeni Gusev IBM		
	17:00	Gian-Marco Rignanese Leuven University		

*** POSTERS SHOULD BE PLACED ON MONDAY MORNING AND DISCUSSIONS WILL OCCUR DURING THE COFFEE BREAKS. ALL POSTER CONTRIBUTERS WILL HAVE 5 min TO GIVE AN ORAL PRESENTATION OF THEIR WORK.**

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14. ABSTRACT

The Proceedings for International Workshop on Device Technology: Alternatives to SiO2 as Gate Dielectric for Future Si-Based Microelectronics, 3 September 2001 - 5 September 2001

This meeting focuses on different aspects concerning electrical, structural and physico-chemical characterization of alternative oxide materials, the so called high-K dielectrics, which are being considered as replacements for SiO2 as gate dielectrics in ultra-large scale integration devices. Recent progress in sub-2 nm oxide and oxynitride gate dielectrics will be also approached, as they constitute the present stage of semiconductor technology. Finally, the emerging field of oxide, oxynitride and alternative oxide films on SiC will also compose the program. It is the purpose of this Workshop to establish a vivid and quite informal meeting for discussing the subjects in the presence of leading researchers from major semiconductor device manufacturers, research centers and university laboratories.

15. SUBJECT TERMS
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INTERNATIONAL WORKSHOP ON DEVICE TECHNOLOGY

Alternatives to SiO_2 as Gate Dielectric for Future Si-Based Microelectronics

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Purpose and Scope

This is the third of a series of bi-annual International Workshops on atomic scale understanding of future trends in ultra-large scale integration (ULSI) devices in Si-based microelectronics. The first Workshop in the series was held in Saint-Petersburg in 1997 and the second in Shanghai in 1999. This third Workshop will focus on different aspects concerning electrical, structural and physico-chemical characterization of alternative oxide materials, the so called high-k dielectrics, which are being considered as replacements for SiO_2 as gate dielectrics in ULSI devices. Recent progresses in sub-2 nm oxide and oxynitride gate dielectrics will be also approached, as they constitute the present stage of semiconductor technology. Finally, the emerging field of oxide, oxynitride and alternative oxide films on SiC will also compose the program. It is the purpose of this Workshop to maintain the spirit of the two previous ones, establishing a vivid and quite informal meeting for discussing the subjects in the presence of leading researchers from major semiconductor device manufacturers, research centers and university laboratories.

I - Electrical characterization of MOS structures using novel high-k oxides on Si. Deposition and growth methods of high-k gate dielectrics on Si. Atomic scale understanding of thin and ultrathin films of high-k oxides and their interface with Si. Electrical characterization and atomic scale understanding of stability and post-deposition annealing of high-k materials on Si.

II - Growth, deposition and atomic scale characterization of sub-nanometric silicon nitride, oxide and oxynitride films as intermediate layers between high-k oxides and Si substrate.

III - State of the art on growth, electrical, and physico-chemical characterization of sub-2 nm silicon oxide and oxynitride films on Si.

IV - Electrical characterization and atomic scale understanding of oxide and oxynitride films on SiC.

The Rio Grande o Sul State Government is in a process of establishing a Research and Development Pole in Microelectronics and Informatics Technology - CEITEC - whose base is the town of Porto Alegre. Thus, the Workshop provides an unique opportunity to meet this effort and getting associated to it.

Proceedings

This Workshop was kindly included into the Materials Research Society – MRS – official workshop series. Therefore the Proceedings will be published as regular MRS Proceedings. Instructions for preparation of manuscripts can be obtained in the Workshop website.

Program

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	16:30	Alfredo Pasquarello IRRMA	POSTER SESSION (5 min ORAL PRESENTATION)*	Shashi Karna USAF
	17:00			Concluding Remarks

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Social, Cultural, and Gastronomical Program of the International Workshop on Device Technology

ALL THE ACTIVITIES OF THIS PROGRAM, EXCEPTING THE WELCOME PARTY, WILL TAKE PLACE WITHIN SHORT WALKING DISTANCES FROM THE WORKSHOP SITE (Hotel Embaixador).

Sunday, September 2nd - Venue

From 11:00 AM to 4:00 PM
Walk around the open handicraft and flea market at Rua José Bonifácio and in the river-side at Ponta do Gasômetro (possibility of boat tour in the Guaiba lake) meeting local people. Try to see youngsters playing "capoeira".

6:00 PM - Welcome Party
Adriano Macedo and Sonino Canhoto playing music from the Pampas (Gaucho Folklore) with dances and other attractions at the Galpão Crioulo of TERMOLAR Inc. . TERMOLAR Choir singing Southern Brazilian music.
Gaucho-style meat barbecue (churrasco) served with Southern Brazilian wines and chimarrão (gaucho traditional tea).

Monday, September 3rd

12:00 PM
Chorinhos (sub-urban music from Rio de Janeiro) with Plauto Cruz (flute) and João Pernambuco (guitar) at the old Chalet da Praça XV, a landmark of nineteenth-century romantic Porto Alegre.
Lunch at the old Chalet da Praça XV.

8:00 PM
Brazilian Popular Music (bossa nova, samba, etc...) with "D'Quina Pra Lua", a women ensemble of voices and instruments presenting the best of Brazilian popular music of the last four decades, played at the Foyer of Teatro São Pedro.
Bahian Food (Afro-Brazilian Cuisine).

Tuesday, September 4th

12:15 PM
Bolivian-Peruvian-Chilean music, voices and dances performed with typical instruments of those countries around the Andes Mountains region at the Mezanino of the Market Place in the Old Port Area.
Sea-food lunch at the Mezannino of the Market Place in the Old Port Area.

7:00 PM
"High Civilizations of Pre-Hispanic Meso- and South-America", a talk given by Israel Baumvol at the Conference Theater of Casa de Cultura Mario Quintana.
Chilean, Argentinean, Uruguayan, and Southern Brazilian Wines Sampling.

8:00 PM
Feijoada (Brazilian National Dish) and Caipirinha (Brazilian National Drink) at Café Concerto, Casa de Cultura Mario Quintana. Continuation of Wine Sampling.
Samba, pagode, etc ... played by Nanci Araújo and her band.

Wednesday, September 5th

12:15 PM
Lunch at City Hotel.

A LIST OF OTHER ACTIVITIES AND RESTAURANTS WILL BE AVAILABLE AT THE WORKSHOP SITE (Hotel Embaixador).

Abstracts (Talks)
Listed by order of presentation

INTERNATIONAL WORKSHOP ON DEVICES TECHNOLOGY
Alternatives to SiO_2 as Gate Dielectric for Future Si-Based Microelectronics
September 3-5, 2001, Porto Alegre, Brazil

Materials and interface chemistry of high-K gate dielectrics

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In this work we describe recent results using medium energy ion scattering (MEIS), electron microscopy (TEM), and photoemission methods to examine various metal oxide gate dielectrics[1]. We concentrate on interface behavior as the most interesting electrical and materials behavior is thought to occur there. For example during the growth and processing of metal oxide dielectrics excess SiO_2 is formed at the interface; this reduces the interface electrical defect concentration but lowers the overall capacitance. To develop and understanding of oxygen diffusion and incorporation in ultrathin metal oxide films, we have examined a series of high-K oxide films before and after oxidation in ^{18}O-isotope enriched O_2 using high resolution ion scattering. The first feature that we note is that pure high-K metal oxides show very high oxygen exchange rates throughout the film (relative to SiO_2 or Al_2O_3) when we expose films to O_2 at elevated temperature. This behavior could be expected based on the known high ionic conductivity of these materials, but it has been neither quantified nor reported in ultrathin films. Second, we observe oxygen, that diffuses to the metal oxide – silicon interface, forms an SiO_2 film whose thickness is limited primarily by the temperature of the process and the pre-existing SiO_2 thickness. Our working model is that the metal oxide catalytically dissociates molecular oxygen, incorporating excess atomic oxygen into the metal oxide lattice, diffuses toward the SiO_x/metal oxide interface forming new SiO_2. The rate of SiO_2 formation at this interface is faster than that obtained in normal Deal-Grove behavior in the SiO_2/Si system (with molecular oxygen diffusion and reaction). Third, the metal oxides that we have examined tend to transform from an amorphous state to thermodynamically more favorable poly-crystalline phases at temperatures that are attained during processing (600-1000°C). Two problems associated with the recrystallization are film roughening and increases in leakage current. These and other data are presented with special reference concerning how processing parameters effect interface composition and electrical behavior.

The authors would like to acknowledge useful discussions with our colleagues at Lucent (Agere Systems) and IBM, members of the SRC-FEP team, and the SRC and NSF for financial support.

1. B.W. Busch, W.H. Schulte, E. Garfunkel, T. Gustafsson W. Qi, R. Nieh and J. Lee, "Oxygen exchange and transport in thin zirconia films on Si(100)" Phys. Rev. B 62(20) p13290, 2000.

INTERNATIONAL WORKSHOP ON DEVICES TECHNOLOGY
Alternatives to SiO_2 as Gate Dielectric for Future Si-Based Microelectronics
September 3-5, 2001, Porto Alegre, Brazil

Electrical and physical characteristics of group III and group IV-based high-κ gate dielectrics

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The rapid pace of scaling CMOS technology has led to considerable attention in the area high-κ gate dielectrics. Although high-performance applications have recently shown that scaling to 50 nm gate lengths and beyond may be possible,[1] low-power applications require substantially lower leakage currents. For low-power applications, SiO_2 is not expected to meet these requirements for several reasons, including high leakage current. High-κ materials, which are expected to produce lower leakage currents for the same performance as SiO_2, are therefore critical for allowing the continued scaling of CMOS technology.

Various high-κ materials have been studied for this purpose recently, but it is clear that many important characteristics, which are already well known for SiO_2, have yet to be understood for any high-κ material. Understanding and controlling region at both the channel and gate interface is of critical importance to the success of any high-κ material. In this presentation, we correlate electrical and physical characteristics of several potential high-κ candidates, through several analysis techniques. In particular, we use X-ray Photoelectron Spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR), medium energy ion scattering (MEIS) and high-resolution transmission electron microscopy (HRTEM) to determine the structure of the interface, film composition and morphology of these gate stacks. These analytical techniques allow for surface sensitive probing, along with depth profiling of these ultrathin films. These results are correlated with capacitance-voltage (C-V), current-voltage (I-V) and deep-level transient spectroscopy (DLTS) measurements on electrical devices. In particular, several properties of Al, Zr and Hf-based oxides and pseudo-binary systems will be discussed.

Several of the most critical issues to be resolved for any high-κ gate dielectric include the structure of the interface, fixed charge and dopant diffusion through the dielectric. The interface chemistry can be better understood through a powerful technique using electron energy loss spectroscopy (EELS) in the scanning transmission electron microscopy (STEM) mode of HRTEM.[2] These results will be shown to determine the position of various elements in the first few monolayers of the interface with Si. Issues related to fixed charge in the films, and dopant diffusion through the films will reported through a combination of the above-mentioned techniques.

[1] R. Chau et al., Tech. Dig. Intl. Electron Devices Meet., p. 45 (2000).
[2] D.A. Muller and G.D. Wilk, to be published.

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Diffusion-reaction of oxygen in high-k dielectrics

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Annealings in oxygen-contaning atmospheres are standard processing steps in CMOS technology that gate dielectric films on Si should tolerate after growth or deposition. Thus, diffusion of oxygen through these films as well as possible compositional changes induced by these annealings must be well understood. In this work we report on atomic-scale processes promoted by annealing in O_2 of high-k material thin films deposited on Si, namely Al_2O_3, $ZrSi_xO_y$ and $ZrAl_xO_y$, under O_2 pressures of 7×10^3 Pa and temperatures that range from 600 to 800°C. Results from annealings in vacuum are also reported for comparison. Elemental compositions as a function of depth are obtained using ion beam techniques, such as narrow nuclear resonance profiling with subnanometric depth resolution and Rutherford backscattering spectrometry. In the case of Al_2O_3 films, mobility of O, Al and Si species, as well as formation of Si-Al-O compounds in near-surface regions at temperatures of 700°C and above are observed only after annealing in O_2. A diffusion-reaction model proposed to describe these phenomena is able to semi quantitatively reproduce the profiles of the involved species [see C. Krug, this meeting]. Diffusion of oxygen through Al_2O_3 films is under detailed investigation using thicker films of Al_2O_3 on Si, annealed in 7×10^2 Pa of $^{18}O_2$ for various times. Preliminary results evidence that profiles of incorporated oxygen are complementary error function-like, characteristic of a diffusive behavior. Oxygen diffusion during thermal annealing under 1×10^3 Pa of $^{18}O_2$ is also being investigated in Gd_2O_3 films. These results will also be presented in this meeting [see D. Landheer]. In the cases of $ZrSi_xO_y$ and $ZrAl_xO_y$ films, mobility of Si is observed after annealings in vacuum and in O_2, while Zr remains immobile. Elemental profiles at the surface region of the films evidence Si accumulation in both materials due to the diffusion of Si from the substrate. On the other hand, elemental profiles at the interface region of $ZrSi_xO_y$ films do not seem to change upon both kinds of annealings, while at the interface region of $ZrAl_xO_y$ they evidence an oxygen profile approximately 20% deeper than in the as-deposited sample after oxygen annealing, indicating oxidation of the Si substrate, and Al loss from this region after vacuum annealing, leading to a graded distribution of Al. The near-interface region of $ZrSi_xO_y$ seems to remain unaltered after both annealings, while the near-surface region becomes richer in Si which is oxidized (after O_2 annealing) or not (after vacuum annealing). In the case of $ZrAl_xO_y$, both near-surface and near-interface regions seem to be altered after both kinds of annealings, following approximately the same trends as $ZrSi_xO_y$. In summary, we must not generalize a conduct for dielectrics submitted to thermal annealings since they behave differently. On the contrary, the thermal behavior of each material has to be investigated in detail.

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Oxide additivity rule and network connectivity considerations in the dielectric constant of mixed oxide systems

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The University of Memphis

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According to the oxide additivity rule the molar polarizability of a mixed oxide system $M_xO_yM'_pO_q$ may be written in terms of the individual molar polarizabilities, $\alpha_m(M_aO_b)$ as:

$\alpha_m(M_xO_yM'_pO_q) = A\ \alpha_m(M_xO_y) + B\ \alpha_m(M'_pO_q)$

so that the dielectric constant is approximately given by:

$$\varepsilon = \{1 + [8\pi/(3V_m)]\ \alpha_m(M_xO_yM'_pO_q)\ \}/\{1 - [4\pi/(3V_m)]\ \alpha_m(M_xO_yM'_pO_q)\}$$

This formula is found to describe the experimental dielectric constant of mixed oxide system within a few percent in a large number of cases. Note that the molecular volume, V_m, of the alloy appears in the formula and the denominator has a singularity if $[4\pi/(3V_m)]\ \alpha_m(M_xO_yM'_pO_q) = 1$. Application of this formula to the derivation of the dielectric constant in mixed oxide systems such as $ZrO_2 + SiO_2$, $ZrO_2+Y_2O_3$, $Ta_2O_5 + TiO_2$ and $Ta_2O_5 + Y_2O_3$ is demonstrated. Apparently anomalous behavior of the dielectric with alloy composition, such as that found in the case of $ZrO_2 + SiO_2$, is discussed in terms of the importance of the molar volume, V_m. It is argued that network connectivity plays a dominant role in determining the molar volume and in consequence, the dielectric constant. Two examples of the effect of change of bonding from fourfold to sixfold coordination in silicate systems are given. On the basis of these considerations we suggest that it should be possible to "engineer" high dielectric constant oxide alloys by choosing components where the "impurity" (taken to be a highly polarizable compound) involves much larger connectivity than the host which provokes substantial reduction in molar volume and hence, dielectric constant enhancement.

atoms. Finally, the model provides a new approach for the optimization transition metal silicate and aluminate alloy compositions for advanced Si devices.

Supported by the ONR, AFOSR and the SEMATECH/SRC Front End Processing Center
[1] GD Wilk et al., J. Appl. Phys. 87, 484 (2000).
[2] HB Gray, *Electrons and Chemical Bonding*, (WA Benjamin, Inc., NY, 1964), Chap. IX.
[3] J Robertson, J. Vac. Sci. Technol. B 18, 1785 (2000).
[4] G Lucovsky and GB Rayner, Appl. Phys. Lett. 77, 2912 (2000).

INTERNATIONAL WORKSHOP ON DEVICES TECHNOLOGY
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Modeling the growth kinetics of ultrathin films of silicon oxynitride and high-k dielectrics

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Since the earliest days of Si-based MOS device fabrication, an accurate description of the kinetics of thermal growth of SiO_2 films on Si was essential. Control of the gate oxide film thickness through processing parameters as growth temperature and time and O_2 partial pressure to comply with design specifications became also essential to meet scaling targets. Beyond the limits of SiO_2 as gate dielectric in ULSI devices, the capability to foresee the gate dielectric film thickness will always be essential, either with regard to silicon oxynitrides (now in the production line) or to a high-K material. Apart from fulfilling the immediate need to predict such gate dielectric film thickness, for which an empirical law is by all means sufficient, a kinetic model usually provides useful insight into the physics and chemistry of the materials in question.

A phenomenological model of the kinetics of thermal oxidation of Si was originally proposed by Deal and Grove [1], who assumed steady-state diffusion of an oxidant species through SiO_2 to react with Si at a sharp interface. This resulted in a well-known linear-parabolic relationship between SiO_2 film thickness and oxidation time, valid above 30 nm. The thickness domain under 30 nm was then called "anomalous," but it became exactly the one of interest for MOS device fabrication. Many authors modified the original model to describe the "anomalous" regime, usually by introducing fitting parameters not prone to physical interpretation. Therefore, the fitting expressions did not allow evolution in terms of understanding of the Si oxidation process.

A unified description of the Si oxidation process from the earliest stages was recently achieved using diffusion-reaction equations [2]. The model assumes only an oxygenated species diffusing through SiO_2 to react with Si wherever the species meet. Neither a sharp interface nor steady-state diffusion is originally assumed, but under such assumptions, justifiable in the thick-film growth regime, the formulation is shown to yield the solution of Deal and Grove. This could actually be seen as a requirement of the model, given the extensive data confirming the solution of Deal and Grove for oxides above 30 nm. The new model shows interesting scaling properties. All experimental kinetic curves (oxide thickness versus oxidation time), irrespective of growth temperature or O_2 pressure, are shown to collapse to a single universal curve if appropriate units are used. This curve was calculated by numerical solution of a system of coupled, partial differential equations by the method of finite differences. Fitting of experimental data with the model curve yielded the diffusion coefficient for the oxidant species in SiO_2 and the reaction rate for Si oxidation in a variety of experimental conditions.

The model originally proposed for Si oxidation was significantly modified and extended to the thermal growth of silicon nitride from NH_3 [3]. Ultrathin nitride films may be useful as buffers in gate stacks involving high-K materials. Thermal growth using ND_3 may be specially suited due to a low growth rate combined with introduction of deuterium at the gate stack/Si interface. Silicon nitride is alson known to be a much better diffusion barrier than the oxide. In this case the model assumes diffusion of a nitriding species (NH_2) followed by reaction with Si up to the point that stoichiometric Si_3N_4 is formed at the surface. In-diffusion

from the gas-phase is then assumed to stop, but the nitriding species still available in a Si-rich nitride underlayer are allowed to react. Comparing our models, such restriction is the origin of the difference between kinetics of silicon nitridation and silicon oxidation. Numerical solutions of the model equations yield kinetic curves in very good agreement with experimental data, reproducing the characteristic feature of self-saturating growth.

A model intermediate to those proposed for the growth of SiO_2 and Si_3N_4 can be applied to the technologically relevant, timely problem of SiO_xN_y thermal growth using NO. The general approach used in such modelling is expected to be useful in the future for a description of the behavior of different gate dielectric materials upon thermal annealing. One recent accomplishment was a description of the system $Al_2O_3/SiO_2/Si$ upon rapid thermal annealing in O_2 [4]. Ion beam analysis and X-ray photoelectron spectroscopy evidenced transport and chemical reaction involving Al, O, and Si, whose depth profiles were qualitatively reproduced using a diffusion-reaction model. The assumption that O triggers the whole process was seen to be in agreement with experiment, which showed no evidence of atomic transport or chemical reaction upon annealings in vacuum. The time-evolution of the interfacial oxide thickness and/or of the Al_2O_3 modification will eventually be calculated.

[1] B. E. Deal and A. S. Grove, J. Appl. Phys. **36**, 3770 (1965).
[2] R. M. C. de Almeida, S. Gonçalves, I. J. R. Baumvol, and F. C. Stedile, Phys. Rev. B **61**, 12992 (2000).
[3] R. M. C. de Almeida and I. J. R. Baumvol, Phys. Rev. B **62**, R16255 (2000).
[4] C. Krug, E. B. O. da Rosa, R. M. C. de Almeida, J. Morais, I. J. R. Baumvol, T. D. M. Salgado, and F. C. Stedile, Phys. Rev. Lett. **85**, 4120 (2000).

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Silicon oxynitride as alternative gate dielectric for advanced microelectronics

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In order to improve the device performance, gate oxide has been scaled aggressively for advanced technology. There are two major challenges as gate oxide thickness decreases: (1) the gate leakage current through the gate oxide increases significantly, and (2) boron penetration in surface-channel PMOSFETs with P^+ gate increases significantly. One efficient way to reduce leakage current is to use a gate dielectric with high dielectric constant, which provides a physically thicker film for the same electrically equivalent SiO_2 thickness. Metal oxides such as TiO_2 and Ta_2O_5 conventionally used as DRAM capacitor dielectrics with very high dielectric constant have been considered as CMOS gate dielectrics to address above-mentioned problems. Although progress has been made, it is challenging to grow ultra-thin metal oxide with stable electrical and physical properties through an entire device fabrication process. Recently, medium dielectric constant metal oxides such as HfO_2 and ZrO_2, and Al_2O_3 have been studied. Although the results of leakage current reduction with very thin equivalent oxide thickness (EOT) were impressive, there is still a long way to go before we can implement it for mass production. Integration of these metal oxides into conventional CMOS flow is a big challenge. On the other hand, silicon nitride is an attractive candidate for this purpose due to its relatively high dielectric constant, extensive usage in IC industry, and relative ease of integration into conventional CMOS flow. Further, nitride is an efficient diffusion barrier which can minimize the boron penetration problems encountered for P^+ gate integration. However, conventional LPCVD nitride has a poor interface with silicon and is leaky due to a high trap density in the film. Therefore, conventional LPCVD nitride is not an attractive candidate for a future gate dielectric for ULSI. Recently, a high quality **integrated oxynitride (ION)** film fabricated in a commercially available RTCVD nitride system which is compatible with standard CMOS processing technology was studied. In addition, nitride deposited by Jet vapor Deposition (JVD) and decoupled plasma nitridation (DPN) oxynitride have been studied recently, and have shown encouraging electrical results. In this paper, we will present the results of implementing ION and JVD nitride, and DPN oxynitride as gate dielectrics for devices using a deep-sub-micron CMOS technology with polysilicon gates. Leakage current reduction, boron penetration resistance, and MOSFET characteristics were evaluated. Pushing high quality oxynitride gate dielectric extendibility would be a trend in industry before implementing metal oxide.

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Nitridation of ultrathin thermal oxides by nitric oxide (NO)

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Ultrathin Oxynitride gate dielectrics have shown to possess highly improved material properties as compared to nonnitrided oxides[1]. The major modifications reported are: the formation of a diffusion barrier for boron, a reduced interface defect density and improved degradation behaviour.

The formation of oxynitride films can be obtained by a variety of techniques: the most currently employed are direct growth in a mixed oxygen/N_2O atmosphere, post oxide growth thermal treatment in nitric oxide (NO) or N_2O athmospheres, plasma nitridation or oxide growth on N preimplanted surfaces. These processes produce "oxynitride" films with different properties and nitrogen distributions. We have in particular studied the effects of oxynitride formation by NO thermal treatments, which we believe is a particularly promising approach.

We have recently shown[2-4] that the nitrogen incorporation by this process is limited to a reactive layer at the interface; it has a strong effect on the Pb center concentration as determined by EPR spectroscopy. In particular, thermally stable "Pb center free" - [Pb]<$10^{11}cm^{-2}$- interfaces can be formed without need for hydrogen passivation

Whereas the improved properties of nitrided gate oxides have been clearly evidenced by electrical measurements the microscopic processes giving rise to the N incorporation, the N in-depth and lateral distribution in the oxide, the local bonding configurations and the overall influence of the oxide type are much less known.

We will here mainly present the results obtained for thin (28Å) dry oxides grown by RTO which have been subsequently submitted to nitric oxide (NO) RTN or furnace annealings. We have performed combined Electron Paramagnetic Resonance (EPR), Nuclear Reaction Analysis (NRA), Atomic Force Microscopy (AFM) and X-Ray Photoelectrons Spectroscopy (XPS) studies on thermal oxides of different thickness in order to obtain an insight in the incoroporation mecanism. Different process parameters such as the nitridation temperature, NO pressure and additional postnitridation thermal treatments have been explored.

The Pb centre concentrations were measured by X-band EPR spectroscopy. The total areal densities of N and O incorporated during the oxynitridation were determined by NRA taking advantage of isotopic labeling ($^{14}N^{16}O$ or $^{15}N^{18}O$) [5]. Depth concentration profiles of ^{18}O and ^{15}N with sub-nanometric resolution were performed using the narrow isolated resonances at 151 keV for $^{18}O(p,\alpha)^{15}N$ and at 429 keV for $^{15}N(p,\alpha\gamma)^{12}C$. The formation and distribution of the oxynitrides at the interface has been further studied by AFM on samples on which the oxide had been removed chemically. The bonding configuration of the N atoms has been determined by the analysis of the N_{1s} XPS spectra.

NO treatments in the 700 to 1100°C range at pressures of 20mbar to 1atm can lead to the incorporation of up to a few 10^{15} cm^{-2} nitrogen atoms. They are located mainly in a 10Å thin layer at the interface. The N distribution is inhomogeneous and is modified by subsequent thermal annealings.

The EPR results show that the N incorporation itself is insufficient for the reduction of the interface state density and that a successful treatment requires in addition a thermal relaxation step, which is generally not achieved during RTN treatments. The kinetics of the NO incorporation and the Pb defect reduction as well as the absolute concentrations of eliminated Pb centers and incorporated N atoms are not directly correlated, indicating that the NO is not directly interacting with the interface defects. Intermediate N concentrations are found to be sufficient for the interface defect optimisation.

The oxynitride distribution at the interface was analyzed by AFM and XPS both on as processed and HF etched samples. We observe the formation of Si_3N_4 islands, typically 10 Å high and 100 Å wide. Depending on process conditions both single peak and multiple peak N1s spectra are observed.

Further extension of this process to other semiconductors (6H-SiC/SiO_2) will be discussed.

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Processing and characterization of ultrathin silicon (oxy-) nitride films grown or deposited on silicon and SiO_2 surfaces

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Ultrathin silicon nitride and oxynitride films are becoming increasingly important in the semiconductor industry [1,2]. These films find applications for use in gate dielectric stacks, polysilicon sidewall spacers and diffusion barriers for logic and memory devices. The material, diffusion barrier and electrical properties of these films are strongly dependent upon the growth technique that is employed. Nitrogen concentration and profile, film thickness and uniformity, and film continuity are all important issues to understand when selecting the appropriate film for a desired application. Silicon (oxy)nitride films used in the semiconductor fabrication process continue to be grown/deposited thinner and thinner as device dimensions continue to shrink.

In this work, we have compared the growth kinetics, nitrogen composition and profile, morphology and electrical characteristics of silicon nitrides and oxy-nitrides prepared by several techniques. These include rapid thermal (RT) processes such as N_2O [3], NO, $NO+O_2$, and NH_3 (oxy)nitridations as well as ultra-thin LPCVD and RTCVD and nitride and oxy-nitride deposition processes and films deposited by plasma-assisted methods. The following measurement techniques [4] were used to characterize these films: ellipsometry, nuclear reaction analysis (NRA), medium energy ion scattering (MEIS), atomic force microscopy (AFM) and C-V and I-V electrical characterization of poly-Si gated devices. With a thorough understanding of the growth behavior, and material properties of ultra-thin silicon (oxy)nitride films grown by different techniques, we can tailor the film thickness, nitrogen concentration and profile to optimize the materials diffusion barrier and electrical properties for desired applications.

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Chemical structures of oxynitrides/Si(100) interface

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Extensive studies have been performed because silicon oxynitrides are desirable gate dielectrics in MOS devices, due to their high reliability and ability to suppress boron penetration. However, the oxynitrides/Si interface structure has not been clarified yet. This is because the detection of the nitridation-induced changes in Si 2p photoelectron spectra is extremely difficult and the oxynitrides/Si interface structures have been studied only from the angle-resolved N 1s spectra. It is the purpose of the present paper to clarify the chemical structures of oxynitride/Si(100) interface from the measurements of Si 2p photoelectron spectra and angle-resolved N 1s spectra.

Oxynitride films containing nitrogen atoms with four concentrations were prepared by annealing the silicon oxide films, which were formed on Si(100) by the wet oxidation, in NO ambient at 900°C during four annealing times. A silicon oxide film was also formed on Si(100) at the same wet oxidation condition. Equivalent oxide thicknesses of both oxynitride films and a silicon oxide film were 2.7 nm. Si 2p spectra and angle-resolved N 1s spectra excited by AlKα radiation arising from these films were measured by high resolution and highly sensitive ESCA-300.

It was found from the determination of the nearest neighbors of a N atom from N 1s photoelectron spectra that a N atom is mostly bonded with three Si atoms. It was also found from the angle-resolved N 1s spectra that N atoms localize mostly at the interface. The distribution of N atoms in addition to that of intermediate oxidation states in depth direction is also confirmed on an atomic-scale by applying maximum entropy method to the analysis of angle-resolved Si 2p photoelectron spectra. Here, the effect of elastic scattering of Si 2p photoelectrons in oxynitride films was considered. It was found from the determination of the nearest neighbors of a Si atom bonded with a N atom from nitridation-induced changes in Si 2p spectra that a Si atom is mostly bonded with three oxygen atoms and one N atom.

The nearest neighbors of a N atom, the nearest neighbors of a Si atom bonded with a N atom, and the localization of the N atom at the interface described above uniquely determine the bonding configuration of the N atoms in the oxynitride films. Namely, a N atom is bonded with two Si atoms at the interface and one Si atom bonded with three oxygen atoms located into the overlayer. The nitridation-induced surface and interface roughness were also found to affect on the oxynitride/Si(100) interface structures.

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Oxygen diffusion in amorphous SiO_2: A first-principle investigation

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The diffusion of an oxygen species through a thin film of amorphous SiO_2 is one of the fundamental steps of the silicon oxidation process.Since the model proposed by Deal and Grove, it is generally believed that molecular oxygen is the transported species. However, recent experimental results have raised doubts on the accumulated evidence in favour of this interpretation [1].Furthermore,theoretical studies,based on sophisticated first-principles calculations on α-quartz, show that alternative diffusion mechanisms are energetically competitive with the di .usion of interstitial molecular oxygen [2,3].

In this work, we address the issue of the transported oxygen species in amorphous SiO_2 To this end,we used a series of structural models for this material.These models were obtained either by .rst-principles or classical molecular dynamics. They all consist of periodic structures of corner-sharing tetrahedra with structural properties which compare well with available diffraction data. Using first-principles approach based on gradient corrected density functionals, we studied the energetics of different oxygen species. We considered both atomic and molecular oxygen,in interstitials or incorportated in the SiO_2 network.These calculations revealed that interstial O_2 is the most stable species. In fact, the oxygen molecule is repelled by the network and the energetics is found to be determined by the size of the interstitial. Since the average interstitial size in amorphous SiO_2 is much larger than in α-quartz, these results are fully consistent with those obtained previously with similar methods [2,3].

Having established the most stable species, we considered pathways for diffusion. To address the large variety of possibilities in an amorphous network,we matched a scheme based on classical interaction potentials to our first-principles results. For a few cases, we calculated the energy profile of the transition between neighboring local minima with both the first-principle and the classical scheme.The good agreement validates the use of the classical scheme. Using this scheme,we then performed extensive calculations in order to characterize the potential landscape of O_2 in amorphous SiO_2. In particular, this provided us with energy distributions of local minima, saddle-points,and transition barriers.

To study the long-range di .usion properties,we mapped these distributions onto a simpli .ed cubic lattice model, in which neighboring lattice sites,representing local minima, are connected by transition barriers. The distribution of branches out of a lattice site was taken to reproduce the situation in our models of amorphous SiO_2 . This could be achieved by attributing an in .nite energy to some transition barriers.The other transition barriers were assigned according to the distribution found for our models of amorphous SiO_2 . By studying the percolation within a Monte-Carlo approach, we finally extract an activation energy of about 1.2 eV,in very good agreement with experimental estimates for oxygen diffusion. These results fully support a diffusion mechanism in which the transported species is molecular oxygen.

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Development of epitaxial oxides on silicon by molecular beam epitaxy for CMOS gate dielectric applications

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One of the main problems facing the semiconductor industry to the continuing reduction in the size of Si CMOS devices, is the scaling of the SiO_2 (high-k) gate dielectric. Presently SiO_2 is being used but at thickness below 20 Å, it suffers from high tunneling leakage current and reliability problems. Alternative high-k materials to replace SiO_2 need to be developed as soon as possible. The alkaline earth oxides such as barium strontium titanate ($Ba_xSr_{1-x}TiO_3$) have a substantially higher dielectric constant than SiO_2 and are ideal candidates for gate dielectrics. Because of the higher dielectric constant a physically thicker layer can yield an equivalent oxide thickness of < 20 Å, thereby eliminating the leakage problems experienced with ultra-thin SiO_2. These oxides also exhibit ferroelectric behavior and their use as the gate dielectric on Si can be exploited in the realization of a single transistor memory element.

In this presentation we will present our approach in depositing high quality epitaxial $Ba_xSr_{1-x}TiO_3$ ($0 \leq x \leq 1$) layers on silicon with low leakage and effective oxide thickness <10 Å. Growth is carried out in a turbo-pumped MBE system with base pressure < 5×10^{-10} mbar and capable of deposition on 8" wafers. Fluxes and growth rates are calibrated using reflection high energy electron diffraction (RHEED) intensity oscillations and the surface is monitored in real time, also using the RHEED technique. Growth is initiated on a (2x1) reconstructed Si(100) surface with fluxes of Ba, Sr, Ti and oxygen at $200 < T_{growth} < 800$°C and oxygen levels up to 10^{-5} mbar and proceeds with a (1x1) reconstruction. Ex-situ analysis of the oxide layer indicate that growth proceeds with a 45° rotation of the lattice with respect to the silicon lattice to accommodate the large lattice mismatch between the oxide layer and silicon. Atomic simulations have been extensively carried out to determine the structure of the oxide/Si interface that was subsequently confirmed by high resolution transmission electron microscopy studies. The oxide films grown on (100) silicon are (100) orientated as determined by x-ray diffraction and AFM measurements show rms roughness < 1Å.

Electrical measurements on $SrTiO_3$ capacitors fabricated on wafer using platinum gate electrodes demonstrated leakage as low as 10^{-5} A/cm^2 for equivalent oxide thickness of 15 Å. In fact, for the same equivalent oxide thickness, the leakage current for MOSCAPs using epitaxial $SrTiO_3$ layers is more than 5 orders of magnitude lower than for SiO_2. Interface state densities in the mid 10^{-10} cm^{-2} eV^{-1} were also measured. Both p- and n- channel MOSFET devices were fabricated using $SrTiO_3$, the results for these will be presented.

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Problems and expected solutions for the gate oxide thinning in miniaturized CMOS ULSI devices

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Progress of MOS LSI has been achieved by continuous downsizing of its components such as MOSFETs. In fact, MOSFETs have been miniaturized significantly over the past 30 years. Its lateral and vertical dimensions have shrunk 2 orders of magnitude for the period. Thanks to the miniaturization, the number of components in a DRAM has increased more than 100,000 times and clock frequency of a MPU has increased more than 2,000. It can be said that the downsizing of the components has driven the tremendous development of LSIs.
However, the downsizing of CMOS devices is now facing severe difficulties at 0.1 μm technology node because of various expected limitations. For, example, SiO_2 has been used almost solely as the material for the gate insulator since the realization of MOSFETs in 1960. Recently, thinning of the gate oxide has proceeded very aggressively and the gate SiO_2 film thickness has already plunged into the direct-tunneling regime and reached 2 nm in the product level. Now, further thinning of the gate SiO_2 dielectrics becomes close to its limit and becomes the most critical issue for the development of next generations of CMOS LSIs.

In this paper, current problems of the ultra-thin gate dielectrics are discussed from the different viewpoints of various LSI applications. In order to overcome the problems, introduction of new materials and device structures have been seriously investigated. Future CMOS gate dielectric technologies such as ultra-thin direct-tunneling SiO_2 and new high-k dielectrics are explained technologies

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Defect generation in ultra-thin high permittivity gate dielectric layers

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The generation of defects during the electrical stress of MOS devices with ultra-thin SiO_2/ZrO_2 gate dielectric stacks is studied. A polarity dependence for the defect generation is observed through the time-dependence of the current density variation $\Delta J_G=J_G(t)-J_G(0)$ during constant gate voltage stress as well as the shift in the capacitance-voltage characteristics induced by the electrical stress. This polarity effect is not consistent with the anode-hole injection model, but can be consistently explained by assuming the release of hydrogen close to the SiO_2/ZrO_2 interface, followed by the transport and trapping of hydrogen in the gate dielectric, resulting in the creation of hydrogen-induced bulk neutral traps N_{ot} and fixed positive charge N_f. The injected-electron energy dependence of N_{ot} and N_f is shown to be consistent with the energy dependence of the hydrogen release cross-section. Finally, the time-dependence of ΔJ_G is modelled within a dispersive transport model, assuming that the defects responsible for the current density variation are induced by the random hopping of H^+ ions in the gate dielectric stack. It is shown that the stress-voltage and thickness dependence of ΔJ_G can be quite well reproduced by this model.

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Gadolinium oxide and amorphous silicate films deposited on Si(100) by electron-beam evaporation: stability and diffusion

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Since the chemistry of yttrium, lanthanum, and the lanthanides (rare-earths) are similar, gadolinium oxide and silicate films should have many properties in common with their La and Y counterparts. However, the reduction in ion radius with increasing atomic number due to the "lanthanide contraction" results in an ionic radius for Gd between that of La and Y. The variation in ionic radius impacts the polarizability, the oxide crystal structure and the crystallization temperature of the amorphous silicates. To investigate the potential of amorphous gadolinium oxide or silicate films for high-κ dielectrics, films were deposited on singular Si(100) substrates from a rod-fed electron beam evaporator using pressed-powder Gd_2O_3 or Gd silicate targets. The silicates were sintered mixtures of SiO_2 and Gd_2O_3 in the molar ratio of 16:84 or 50:50. The oxide films were stoichiometric Gd_2O_3, as determined by Rutherford backscattering and had a dielectric constant at 100 kHz of 16. Studies on the silicate films focused on those with the composition close to that of gadolinium orthosilicate (Gd_2SiO_5). Surprisingly, these also had a dielectric constant of 16 at 100 kHz. Capacitance-voltage measurements indicate an equivalent oxide thickness (EOT) of 11.0 Å for a vacuum-annealed film 45 Å thick with composition $GdSi_{0.56}O_{2.59}$. The same film had a low leakage current of approximately 5.7×10^{-3} Acm^{-2} at +1V, a reduction of 8.7×10^{4} compared to current density estimates of SiO_2 films with the same specific capacitance. Atomic force microscopy indicated that further current reductions could be expected for smoother films. Transmission Electron Microscopy (TEM) and Electron Energy-Loss Spectroscopy showed that pure oxide films 7-13 nm thick annealed in oxygen consisted of three distinct layers, an interfacial silicon oxide layer next to the substrate, a second amorphous oxide layer containing Si, Gd, and O above this, and a polycrystalline Gd_2O_3 layer on top. Annealing in O_2 reduced the leakage currents, increased the thickness of the SiO_2 layer, and increased the grain size of the top Gd_2O_3 layer. Narrow Nuclear Resonance Profiling (NRP) of oxygen and silicon using the $^{18}O(p,\alpha)^{15}N$ and $^{29}Si(p,\gamma)^{30}P$ nuclear reactions on the Gd_2O_3 films allowed to verify different atomic transport processes occurring during annealing in oxygen.By Fourier Transform Infrared Spectroscopy (FTIR) it was possible to follow the growth of an interfacial layer in 30-40 nm thick films annealed in oxygen at 800-900 °C. For oxide films a peak at 1060 cm^{-1}, characteristic of SiO_2, increased but quickly saturated. Another, broader peak near 920 cm^{-1} is indicative of suboxide or silicate growth. For the silicate films, part of the changes resulting from oxygen annealing could also be ascribed to the growth of an interfacial oxide. TEM and FTIR analysis showed that the silicate films were amorphous as-deposited and remained amorphous when annealed to temperatures as high as 1050 °C. The high crystallization temperature and dielectric constant of gadolinium silicate make this material a promising alternate gate dielectric. The films are stable in the thermodynamic sense but more work needs to be done to suppress the effects of O and Si diffusion at the interface.

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Characterization of ultrathin gate dielectrics on silicon by photoelectron spectroscopy

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A fundamental understanding of chemical and electronic structures of thin films of high-dielectric-constant (high-k) materials on silicon and their interface properties is of great importance in using the materials as alternative gate dielectrics for sub-100nm CMOS devices which require a high-reliable gate dielectric with a SiO_2 equivalent thickness below ~1.5nm. In this paper, we focus on the determination of energy band alignments and gap-states distributions for heterostructures of practically-thin high-k dielectrics such as Ta_2O_5, Al_2O_3 and ZrO_2 on Si(100).

We first demonstrate that energy bandgaps of thin dielectrics are determined by measuring energy loss spectra of core-level photoelectrons[1-3]. From the onsets of O1s energy loss spectra of the films, the bandgap values were measured to be 4.65-4.75eV for 4.5~10nm-thick amorphous Ta_2O_5, 6.95eV for 3~10nm-thick amorphous Al_2O_3 and 5.5eV for 2.6~10nm-thick amorphous ZrO_2.

The valence band lineups between the high-k dielectrics and metals or Si(100) have been determined from the analysis of valence band spectra for thin high-k dielectrics formed on Si(100). By deconvoluting the measured valence band spectra for the thin heterostructures using the valence band density-of-states (DOS) curves separately measured for thick high-k dielectrics and hydrogen-terminated Si(100), the valence band offsets between Si(100) and amorphous Ta_2O_5, Al_2O_3 or ZrO_2 were obtained to be 3.25, 3.75 and 3.15±0.05eV, respectively, which are consistent with theoretically predicted values[4]. The energy band diagrams for metal/high-k dielectrics/Si(100) systems have been explicitly derived by considering the measured bandgaps, valence band lineups, electron affinities of the dielectrics and metal work functions determined by photoelectron yield measurements.

We also demonstrate that total photoelectron yield spectroscopy (PYS) is a useful tool to quantify the energy distributions of electronic defect states in ultrathin gate dielectrics as well as at the dielectric/Si(100) interfaces over entire Si bandgap without gate formation [3-5]. The defect state density in Ta_2O_5, or ZrO_2 films evaporated on Si(100), which is as high as ~$10^{17}cm^{-3}eV^{-1}$ even at an energy near Si midgap, is decreased down to the order of $10^{16}cm^{-3}eV^{-1}$ by 500°C annealing in dry O_2, while the defect states near the interface are increased significantly to midgap densities higher than ~$5x10^{12}cm^{-2}eV^{-1}$ presumably because an SiO_2 or SiO_x:Zr interfacial layer (~1.7nm in thickness) is formed at a temperature as low as 500°C.

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Gate electrode selection process for advanced silicon devices

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In the gate electrode selection process, workfunction, thermal stability and gate depletion are the critical parameters that need to be satisfied. In our studies we have investigated a) elemental metals, b) metal nitrides, c) metal oxides and d) metal alloys as gate electrodes on SiO_2 and high-K dielectrics, such as Y_2O_3, Al_2O_3, Ta_2O_5, ZrO_2, HfO_2. Although, elemental metals have found to exhibit a wide range of workfunction values (3eV to 6eV), obtaining their thermal stability is problematic. We have found that several material properties such as free energy of oxide formation, oxygen solubility, diffusion barrier properties and film microstructure can be used as predictors of stability. Since electronegativity, which is related to free energy of formation, is proportional to its workfunction, elemental metals with lower workfunctions have problems with stability. For e.g., metals such as Ta, Ti, Al, Zr, Hf are inadequate for gate application under conventional process flows since they react with the underlying dielectric. The challenge lies in finding low workfunction metals, which also offers thermal stability. One option to achieve this is to introduce N in metals which have low workfunctions. It has been shown from Cu barrier layer studies that the presence of N can effectively retard reaction rates, provide better diffusion barrier properties and result in smoother microstructures. The use of N in metal can then be advantageous provided that the workfunction is not increased significantly. In our work, we have demonstrated that the addition to N in Ta films indeed improves their thermal stability with a small tradeoff of ~0.2eV larger workfunction and these results will be presented.

Elemental metals with larger workfunctions provide intrinsic stability due to their low free energy of formation. Elements such as Ru, Pt, Ir, Ni, Co are all stable on most dielectrics under consideration today. In our work, we have focused on Ru gates since they do not suffer from the adhesion problems typically encountered with Pt and Ni gates. Moreover, Pt gates have high oxygen conductivity. We have obtained excellent thermal stability of Ru gates on SiO_2 up to 800°C, the highest temperature studied in our lab. In addition, Ru also offers an exciting opportunity that its oxide is also an intrinsic conductor with low resistivity, high carrier concentration and excellent diffusion barrier properties. Its investigation as the bottom electrode in high-K DRAM research lends strength to its potential. In our work, we have and continue to analyze RuO_2 both on SiO_2 and various high-K dielectrics with very promising and exciting results. Beyond the scope of elemental metals, conducting metal oxides and metal nitrides, there is another set of materials that can offer workfunction and thermal stability solutions. This set of materials deals with alloys. In our work, we have begun the exploration of alloys such as $TaSi_xN_y$ and have found that these films resulted in workfunctions that are 4.2-4.27eV, appropriate for NMOS devices. These workfunction values are different from $TaSi_2$ and this is attributed to a Ta/Si ratio of ~1 of our films. We have also investigated the high temperature stability of these films, and excellent EOT stability is observed up to anneal temperatures of 1000°C. The results of these gates on both SiO_2 and high-K dielectrics will be discussed.

The properties of the above metals will be discussed using both, thermodynamic, electrical and physical characterization data. The role of excess oxygen residing in the high-K dielectric on the overall gatestack stability will be discussed. Potential options for engineering both the bottom and top interface to maximize EOT and V_{FB} stability will also be presented.

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Growth and characterization of SiC-SiO_2 interfaces

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Silicon carbide is the only wide band gap semiconductor that has a native oxide, and metal-oxide-semiconductor field effect transistors (MOSFETs) have been fabricated using both the 4H and 6H polytypes of SiC. The 4H polytype has higher bulk carrier mobility, and is hence the polytype of choice for power MOSFET fabrication. However, reported channel mobilities for 4H n-channel, inversion mode devices are substantially lower than 6H-MOSFETs. The poor performance of 4H devices is attributed to a large, broad interface state density located at approximately 2.9eV above the valence band edge in both polytypes. For 6H-SiC (E_{gap} ~ 3eV), these states lie mostly in the conduction band, and do not affect the inversion channel mobility. However for 4H-SiC (E_{gap} ~ 3.3), substantially more of these interface states lie in the band gap where they act to reduce channel mobility through field termination, carrier trapping and Coulomb scattering. It has been proposed that interface states in SiC/SiO_2 structures result from carbon clusters at the interface and defects in a near-interface sub-oxide that is produced when the oxidation process is terminated. We report a complete study of the growth and characterization of these different interfaces. Using TEM/EELS we show the existence of the interfacial carbon and its reduction through oxygenation. We also demonstrate the electrical passivation of the remaining interfacial carbon through NO and NH_3 annealing[1-3]. Detailed measurements of the kinetics of nitrogen incorporation are used to establish the nature of the defect as a function of energy position within the band-gap. These physical measurements correlate strongly with theory, which predicts the position of carbon atomic-size clusters within the band-gap. Finally, channel mobility measurements for n-channel, inversion mode devices indicate that the nitrogen passivation improves the device characteristics[4]. The unique character of SiC, with its various polytypes and band-gaps, provides a unique tool for semiconductor interface science where interfacial chemistry and band-gap can be independently varied.

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Initial oxidation stages of SiC and composition profile of the SiO_2/SiC interface

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SiC is a promising semiconductor in applications involving high-power and high-frequency devices. Besides its interesting electrical and physical properties, it can be thermally oxidized to form SiO_2, the most used and studied dielectric for microelectronic applications. However, the electrical quality of the SiO_2/SiC interface still needs to be improved in order to SiC reach its full potential as a wide band-gap semiconductor. For this reason, the understanding of oxidation mechanisms and composition of SiO_2/SiC structures plays a fundamental role in the development of SiC technology.

In this work, initial stages of oxidation of a 6H-SiC, Si-faced n-type sample were investigated using low energy ion scattering (LEIS) and angle resolved X-ray photoelectron spectroscopy (ARXPS). After chemical cleaning, the sample used in this study was heated in ultra-high vacuum in order to remove possible contaminants and native silicon oxide. The composition of the resulting surface was checked by LEIS evidencing only Si and N. This N content can be a result of the segregation of doping species during the cleaning procedure. We are presently checking this behavior using Medium Energy Ion Scattering. After cleaning, the sample underwent sequential oxidation steps. After each one, ARXPS and LEIS measurements were accomplished. In this way the evolution of the oxidized products was determined. The results evidence that the first oxidation products are silicon oxycarbides (compounds where silicon is bonded to a variable number of O and C) and as oxidation proceeds stoichiometric silicon oxide is formed, mainly at the surface region. The composition of the near-surface region of such thin films is very similar to that reported in previous investigations for the near-interface region when thicker oxides films are grown on SiC.

The depth composition of an oxide grown on Ar^+ bombarded n-type 6H-SiC (0001) sample is also presented, where bombardment was used to enhance the thermal oxidation rate of SiC, which is very low compared to that of Si wafers. The environment of Si atoms was probed as a function of depth by sequential XPS measurements followed by HF etching, carried out until the SiC crystalline surface was reached. AFM measurements of the sample before and after etching were also accomplished, providing textural information of the effects of irradiation and/or oxidation. The results evidenced that in the transition region (~18 nm) between SiO_2 and SiC these species coexist with silicon oxycarbides. These results will be compared to a non-irradiated sample.

In preliminary electrical characterization of these structures it seems that this graded interface is the cause of their poorer electrical properties when compared to Si MOS devices.

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Silicon carbide surface passivation at the atomic scale and Initial Insulator/SiC interface formation

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Surface passivation is a central issue in successful SiC device applications. In this presentation, I will review the most recent findings into the initial SiC surface passivation including understading the oxygen interaction at the atomic scale. The initial oxidation of hexagonal (6H and 4H) and cubic (3C) SiC surfaces is investigated by core level (Si 2p and C 1s) photoemission spectroscopies using 3rd generation synchrotron radiation sources and by atom-resolved scanning tunneling microscopy (STM). The oxide growth is performed by oxygen exposures at surface temperatures from 300 K to 900 K. Unlike silicon surfaces, 6H-SiC and 4H-SiC oxidation is taking place already at exceptionally low oxygen exposures (1 Langmuir). The oxidation rate is significantly enhanced at increasing surface temperatures. The results also indicate that the direct oxidation of the 6H-SiC(0001)3x3 surface leads to SiO_2 formation at low temperatures (800 K) with a non abrupt interface having significant amounts of mixed (Si-O-C) and intermediate (Si^{3+}, Si^{2+}, Si^{+}) oxidation products. In contrast, a C-free and abrupt SiO_2/6H-SiC(0001) interface formation is achieved when a pre-deposited Si overlayer is thermally oxidized at low oxygen exposures and low temperatures (800 K) with little involvement of C atoms located at the SiO_2/SiC interface.

Most significantly, the oxidation process appears to be significantly less efficient on the 4H-SiC(0001) 3x3 surface with smaller amount of oxide products, lower oxidation states and presence of carbon species in the oxide layer. Such findings are especially relevant in view of the higher interface state densities generally observed for oxide/4H-SiC(0001) interfaces.

Oxynitridation is achieved by nitric oxide (NO) interaction of with the Si-rich 3C-SiC(100)3x2 surface. The initial sticking coefficient of the NO molecules is found to be significant already at room temperature with a dissociative adsorption resulting in Si oxynitride products as SiO_xN_y. The amount of oxynitride is significantly increased at surface temperatures of 800 K and above. In addition, temperature is found to favor the formation nitrogen-rich SiO_xN_y oxynitride products leading to SiO_xN_y/□-SiC(100) interface formation.

Finally, the atomic scale oxidation of the 6H-SiC(0001)3x3 surface is studied by atom-resolved STM. Contrary to the case of 3C-SiC, oxygen atoms do not react at surface defect sites but well below the surface which is affected by electronic effects including dark and bright spots forming "flowers" The results reveal that the initial oxidation takes place through the relaxation of lower layers, away from the surface dangling bond, in sharp contrast to silicon oxidation.

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The application of high-K gate dielectrics for high performance CMOS

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Aggressive shrinking of the thickness of SiO_2 -based gate dielectrics in high performance logic ULSI devices below ~2 nm, brings about a number of fundamental problems for continued scaling.[13] Some of the more critical issues relate to reduced dielectric reliability [4-7] and exponentially increasing leakage (tunneling) current with decreasing oxide thickness. [8, 9] This dictates a search for alternative materials (high-K dielectrics) with a dielectric constant higher than that of SiO_2 (3.9). [10, 11]

An important step (and a very challenging task) in the search for high-K gate dielectrics is their physical and electrical characterization [11-13]. The electrical and physical characterizations are, of course, to better understand the material properties and micro-structural aspects of the films in question, including thermal stability, reactivity with silicon etc. and their correlation with electrical properties. Ultimately it is the manufacture and electronic properties of silicon based logic (and/or memory) chips that will determine the usefulness of any of these materials. [12]

In this paper, the application and integration of high-k dielectrics and/or metal gates will be addressed. In particular, the production and characteristics of 80 nm poly-silicon gated n-FETs with an ultra-thin Al_2O_3 gate dielectric [12] will be shown. This work demonstrates the integration of Al_2O_3 gate-dielectrics into a sub 0.1 μm n-MOS process using polycrystalline silicon gates. Devices incorporating Al_2O_3 films with a dielectric constant ε~11 and electrical thickness $t_{qm} < 1.5$ nm have been fabricated. Gate leakage currents are ~100 times lower than those found in SiO_2 films of equivalent thickness. Encouraging device characteristics are shown. Charging due to slow states and/or fixed charge have been shown to be in the 100 mV range which may be related to the somewhat reduced mobility. The room temperature reliability of these devices based upon the values of ß (Weibull slope) and γ (voltage acceleration) suggest that the Al_2O_3 lifetime may exceed that of SiO_2 films.

The use of ALD for the deposition of ultra-thin, high-K, gate dielectrics will be reported. This technique offers excellent uniformity across 200 mm (and larger) wafers, process control, step coverage and low thermal budget. An analysis of physical and electrical properties of ZrO_2, HfO_2, Y_2O_3 and Al_2O_3 [11, 14, 15] will be given. These materials are predicted to be thermodynamically stable on Si and have reasonably high band gap (barrier height) that make them promising high-K candidates for logic (and perhaps memory applications). We found all four materials exhibited gate leakage much lower than that of conventional SiO 2 of the same equivalent electrical thickness (capacitance) and good interface quality (after post-deposition anneals). We further discuss some integration issues, in particular thermal stability.

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Hf-Si and Zr-Si based gate dielectric compounds

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Zirconium and hafnium silicon oxide materials have been found to have key properties as gate dielectrics to replace SiO_2 and/or nitrided SiO_2 gate oxides thus extending CMOS devices beyond the 70nm nodes [1,2]. However a number of very critical issues, such as composition, structural properties, scaling, thermal stability, poly Si/dielectric stability, and many others must be understood and controlled in a manufacturing environment before these new materials can be accepted as gate dielectric candidates. In addition, deposition of these materials for gate dielectric applications is very challenging. The silicon surface conditioning, CVD and/or ALD precursor selection, defect chemistry, and annealing are critical to the success of integrating these materials in the standard CMOS flow. To date much of the published work on high-k gate dielectrics has focused on fabricating capacitors using metal gates. This is believed to be associated principally with difficulties in integrating the high-k materials into a standard CMOS flow using poly silicon as the gate electrode.[3,4,5] Recently, however, significant advancements have been made using HfO_2 and ZrO_2 gate dielectrics with poly silicon gates[6,7] While the results are very encouraging, the suitability of crystalline HfO_2 and ZrO_2 as gate dielectrics still remains to be established. Issues like oxygen diffusivity, dopant penetration, and defect incorporation and segregation at grain boundaries to name just a few, are still not fully characterized.

In this work we report on Hf-Si and Zr-Si based gate dielectrics. These "silicate" materials were selected in an effort to take advantage of the relatively high dielectric constant of the binary metal oxides, the benefits of SiO_2, and the built-in ability to grade the Si/high-k interface with Si-O in order to minimize interfacial traps. The films were characterized by the typical suite of techniques, such as optical techniques, XPS, TEM, AFM, and electrical measurements made on capacitors processed using a standard CMOS flow. Transmission electron micrographs of ~ 3-5 nm "silicate" films capped with poly silicon and annealed at 1000°C for 30 seconds in a nitrogen atmosphere showed that Hf-Si based gate dielectric alloys did not react with the poly Si but Zr-rich films did. The reactions between thin poly silicon and the silicate surface were also analyzed by XPS and the results were in agreement with TEM data, i.e. Zr-rich films reacted with poly whereas none of the Hf containing films did. Hf-Si and Zr-Si based gate dielectrics with varying thickness were used to fabricate nMOS capacitors using a standard CMOS flow, including poly Si electrodes, and anneals up to 1050°C. Zr-Si based films showed high leakage especially for Zr-rich films. On the other hand, Hf-Si based gate dielectric capacitors showed well behaved characteristics including quantum mechanical corrected equivalent oxide thicknesses lower than 1.5 nm and leakage currents of ~ 0.1 A/cm² for a gate bias of 1V over flatband in accumulation. The Hf-Si based dielectric materials studied in our laboratory were found to be thermally stable even when exposed to the full thermal budget used in our standard CMOS capacitor flow. The effective dielectric constant was estimated to be greater than 10 for Hf concentrations ranging from

about 6-10 at%. This brings "silicates" into a range where they can be considered scalable for sub 70 nm nodes.

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High-K Al_2O_3 and Aluminate Gate Dielectrics: Selection of the Ideal Amorphous Composition and Ramifications for Film Growth

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The perceived necessity for amorphous high-K gate dielectric layers, and therefore the thermal budgets they will be exposed to during device processing, determine the selection of aluminate (and silicate) compositions. In this paper we study the crystallization kinetics of Hf and Zr aluminates and silicates covering a wide compositional range. If amorphous layers are indeed necessary, composition and dielectric constant will be constrained. Furthermore, growth techniques for such layers (i.e.,CVD or ALD) will have to be considered. We will also present physical and electrical results on the ALD growth of Al_2O_3 and aluminates.

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First Principles Modeling of High-K Dielectric Materials

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First-principles calculations are performed for high-K gate dielectric materials for bulk and interface systems. Detailed electronic structures and atomic configurations are investigated for metal (Hf and Zr) doped silicate bulk system[1] and a model Si-silicate interface system.[2] Metal atom-interface interactions are elucidated, and this finding sheds a light on recent experimental observations of intermediate silica layer formation. Static dielectric constants of silicate materials are also investigated using the density functional perturbation theory method (Abinit code). We will discuss on recent progresses of the high-k gate dielectric materials simulations.

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Reaction Kinetics at High-k Interfaces

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Unwanted interface layers often result when high-k dielectric materials (including, HfO_2, ZrO_2, Al_2O_3, Y_2O_3, and metal silicates) are deposited on silicon, where unwanted reactions consume the silicon substrate producing low capacitance interface layers. For many of the high-k materials of interest, the interface layers are not expected from simple bulk equilibrium thermodynamics, but rather, result from the non-equilibrium nature of deposition reactions. This indicates that the relative rates of individual elementary reaction steps, and their relation to deposition time and temperature, determine the composition and structure at the interface. Interface reactions at the top interface between the high-k and the gate electrode are also expected to contribute unwanted capacitance to the gate stack, so potential reactions and reaction mechanisms must also be explored for those interfaces. Insight into silicon/dielectric interface reactions can be gained from studies of yttrium silicate formation. Yttrium silicate films with composition close to $(Y_2O_3)(SiO_2)$ and an equivalent silicon dioxide thickness of ~10Å and k ~14 have been formed by a two step deposition process: 1) Y metal is deposited by PVD on clean (100) silicon, then annealed in vacuum to 600°C to form yttrium silicide; and 2) the silicide is removed from vacuum and thermally oxidized at 600°C to 900°C in oxygen. Films were characterized by XPS, IR, MEIS, and IV, CV analysis. Before electrical analysis, samples typically underwent a post-metallization anneal in 90% N_2 and 10% H_2 at 400 °C for 30 minutes. IV analysis shows good leakage (<1A/cm^2 for $V = V_{fb}+1$), and the CV shows evidence for threshold voltage shift indicating fixed charge. The density of fixed charge determined from the flatband shift depends on film thickness, gate metal, and process history, suggesting that charge is not simply fixed at the Si/dielectric interface, but could also result from gate/dielectric interactions.

The rates of metal/silicon and silicide oxidation reactions were characterized, and between room temperature and 900°C the rate of silicon consumption by the metal is found to be thermally activated with a barrier of ~0.30 eV. This can be contrasted with a much larger barrier (3.0eV) observed for metal consumption of SiO_2 under similar process conditions. This means that metals of interest for high-k materials with react favorably with silicon, with only a small thermal barrier, to form a mixed metal/silicon reaction layer that is easily oxidized. We believe that this reaction sequence is what typically results in interface layers typically observed in TEM images of metal oxide on silicon.

We have also characterized reactions between polysilicon and metal oxide materials to begin to understand reactions that proceed at the dielectric/gate interface. We find that when silicon is deposited on ZrO_2 at low temperature (200°C by PECVD) and annealed at 600°C to form polysilicon, XPS shows a thin zirconium silicate layer forms at the interface. This silicate layer is stable upon anneal at 1000°C in Ar. These results are different from what is observed by other groups that saw metal silicide form at the interface when poly was deposited at 600°C on zirconium oxide. We believe that this difference results from the different amounts of water vapor present in the two studies, where the higher OH density at lower temperature promotes silicate formation, whereas smaller OH densities at high temperature promotes silicide formation.

These insights into processes that proceed during dielectric and gate CVD are important to control interface structure during gate stack fabrication for advanced CMOS. To begin to

address interface reactions in gate metal CVD, we have deposited RuO_2 gate metal by CVD in our lab, and we find that films with excellent conformality on 100nm features with 5:1 aspect ratio can be achieved. Interface reactions between CVD metals and high-k dielectrics will also be discussed.

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Physico-chemical and electrical characterization of thin Al_2O_3 layers deposited by Atomic Layer Deposition

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Alternative gate dielectrics have to fulfill various important requirements such as higher K value than SiO_2 (implying a reduction of the leakage current and higher reliability for EOT<2 nm), adequate conduction and valence band offsets, and material compatibility with Si (the interface with the Si must be of extremely high quality in order to still improve device performance). Among the new high K materials, Al_2O_3 (K=9-11) is an attractive candidate for medium term application **[1]**, and low temperature deposited Al_2O_3 is amorphous (its temperature limit for crystallisation was determined around 830°C **[2]**) which is an important prerequisite to reduce impurity diffusion through the layer and the leakage current. Physico-chemical and electrical measurements of thin and ultra-thin Al_2O_3 layers were performed in order to characterize the viability of this material as a gate oxide alternative.

Al_2O_3 layers were deposited by Atomic Layer Deposition (ALD) at low temperature in a Pulsar™ 2000 reactor from ASM Microchemistry Ltd with trimethylaluminum and water as precursors **[3,4]**. The films were deposited either on a ultra-thin SiO_2, or on native oxide or on HF cleaned Si surfaces. The composition and structure of the layers, prepared under various experimental growth or post-deposition annealings conditions, were characterised by complementary physico-chemical techniques such as NRA, NRP, ERDA, SIMS, XPS, AES, MIR and EPR. C(V) measurements were performed to determine the fixed charges, the EOT, and the corresponding K value.

Ultra-thin Al_2O_3 layers deposited on HF cleaned surfaces were investigated by AR-XPS and AES. The Al 2p spectra show only one peak attributed to Al-O bonds (no Al-Al bonds were observed **[5]**) and evidence the stoichiometric composition and the high quality of the Al_2O_3 layers grown by ALD technique with TMA and H_2O as precursors. Post-deposition annealings, known to be necessary to achieve a layer densification **[6]**, were performed in a nitrogen ambient below and above 830°C. At the dielectric/silicon interface, which is initially abrupt (see ref. **[7]**), one observes the growth of an additional intermediate layer, mostly composed of SiO_2; its thickness, which increases with the Al_2O_3 thickness, is strongly related to the hydroxyl groups present in the layers.

Indeed, despite theorical predictions, the two half-reactions **[3]** responsible for Al_2O_3 growth are known to be uncompleted and hydrogen and carbon contamination remain in the as-deposited layers **[8]**. Miller et al. **[9]** speculatively suggested oxygen atoms in excess and/or hydroxyl groups were responsible for the post-deposition annealing induced densification (e.g. a thickness reduction up to 10% was observed at 900°C **[6]**). To answer this question, we performed NRA, ERDA, and SIMS studies. These techniques allowed to

follow the atomic densities as well as the distributions of hydrogen and oxygen atoms as a function of the sample thickness and annealing treatment conditions (temperature, time and ambient). For instance, annealing at 800°C of 45 nm thick Al_2O_3 layers induced important hydrogen desorption whereas no oxygen loss was evidenced. Precise hydrogen depth profiles in the layers, extracted from ERDA and SIMS, will allow us to propose a model for both densification and interfacial layer growth induced by post-deposition annealing.

Our results show further that the K values, extracted from C(V) measurements, as well as the fixed negative charges densities **[6]**, increased with oxide thickness (for ultra-thin films) and annealing temperature. EPR measurements revealed the presence of P_{b0} and P_{b1} centres at as-deposited Al_2O_3/HF cleaned Si interfaces similar to the case of ultra-thin SiO_2/Si interfaces (native or thermally grown oxides). Despite intermediate layer formation during 800°C annealing, little effect was evidenced on the densities of the Pb centres **[10]** which implies that the deposition conditions and silicon surface preparation are the key-point for the dielectric/Si interface quality. Comparison with other high K gate dielectrics grown by the ALD technique will be also discussed at the workshop.

This work has been carried out, in the frame of CEA-LETI/GPS collaboration, with PLATO Organization teams and tools.

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O_2 Diffusion in SiO_2

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Interstitial oxygen plays an important role in the thermal oxidation of SiO_2 (it is important to understand the growth of pure SiO_2 even for oxynitrides, since the nitridation may be performed on pre-oxides), either through the interaction with point defects, or, as many results indicate, as the promoter of the oxide growth after diffusing through the silica network.

We will present results, all based on total energy first principles calculations, for the diffusion of the oxygen molecule in SiO_2. We study the potential energy surface for the hopping of the oxygen molecule between the interstitial sites, both for a triplet as well as a singlet spin configuration. The triplet is always lower in energy, which is consistent with the fact that the oxygen molecules interact only weakly with the oxide lattice. Moreover, the energy barriers are very different, which indicates that the use of spin-polarized approximations is fundamental to understand the properties of this system. We will also present results for interstitial NO and N_2O in SiO_2, and for nitrogen as a substitutional impurity into the silica network. The interaction of these molecules (O_2, N_2O, and NO) with point defects will also be analyzed. All these studies are performed both for the α-quartz as a model for the SiO_2, as well as for an amorphous solid.

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Interpretation of N 1s core-level shifts at nitrided Si(001) surfaces and Si(001)/SiO_2 interfaces: A first-principles study

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Silicon dioxide (SiO_2) is the most extensively used dielectric in the microelectronics industry. However, as the scale of integration increases and the thickness of the dielectric is reduced, the performance of SiO_2 is degraded due to leakage currents and to its permeability to boron and alkali ion diffusion. These problems have stimulated the investigation of a large variety of alternative dielectrics. Because the dielectric which will eventually replace SiO_2 has not yet been identified, nitrided silicon oxides (SiO_xN_y) or even silicon nitrides (SiN_xH_y) appear as interesting ways to meet the requirements of ULSI technology for the near future.

Because the insulating layer required for ULSI devices may be only tens of angstroms thick, the knowledge of the detailed atomic structure of the interface is becoming critical for further improving the performance of electronic devices. Amongst the various experimental techniques, X-ray photoemission spectroscopy (XPS) is particularly sensitive to the various bonding configurations of nitrogen atoms by recording N 1s core-levels. Indeed, XPS has been one of the principal experimental tools for the investigation of both nitrided Si(001) surfaces and nitrided Si(001)-SiO_2 interfaces. However, the interpretation of the experimental spectra in terms of N bonding configurations is not always straightforward and often leads to some controversy. The large variety of techniques which have been used to engineer the nitrogen concentration and composition profiles contribute to this uncertainty. Indeed, different techniques may lead to different bonding configurations and therefore to different values of the core-level shifts.

The purpose of this work is to characterize the bonding configurations of N atoms at nitrided Si(001) surfaces and Si(001)/SiO_2 interfaces. By complementing the experimental XPS studies with a theoretical approach that allows to calculate core-level shifts based on first-principles, we establish a correspondence between bonding environments and N 1s core-level shifts measured in photoemission experiments.

In the case of NH_3 adsorbed Si(001) surfaces, our study provides a clear interpretation scheme for the bonding configurations of the N atoms. According to this scheme, the peaks in the XPS spectra associated to chemisorbed N species can all be interpreted in terms of threefold coordinated N atoms with a varying number of Si and H nearest neighbors, i.e. N-$Si_{1-x}H_x$ with x = 0,...,2. Every additional H atom in the nearest neighbor shell produces a contribution to the N 1s core-level shift of about 0.6 eV to higher binding energies. The XPS spectra do not show a peak at the predicted location for N atoms carrying dangling bonds (Δ=-1.8 eV). We therefore conclude that these defect configurations do not occur in significant amounts during nitridation of the Si(001) surface by NH_3.

At nitrided Si(001)-SiO_2 interfaces, our investigation also provides a clear picture for interpreting XPS spectra. The principal peak results from N atoms threefold coordinated by Si atoms, the large linewidth and the asymmetry being caused by core-hole relaxation and

second nearest neighbor effects. The contribution to the principal peak from N atoms with one H and two Si nearest neighbors cannot be ruled out (Δ=0.4 eV) and will depend on the concentration of incorporated H atoms. The formation of N-O bonds gives rise to additional peaks at higher binding energies and their precise location in spectrum depends on the profile of the N concentration. In fact the shifts depend by as much as 0.8 eV on the overall dielectric environment determined by the distance of the N atoms to the Si substrate. According to our calculations, it also appears clearly that nitrogen atoms carrying dangling bonds do not contribute to the principal peak, as previously suggested in the literature. Instead, such configurations might be at the origin of a peak observed in highly defective samples, at lower binding energies with respect to the main peak.

Among the various bonding configurations, a few are found both at the surface and at the interface and can therefore directly be compared. The $N\text{-}Si_2H$ bonding configurations present shifts of Δ=0.6 and 0.4 eV at the surface and the interface respectively, while for the $N\text{-}Si_2$ configurations (with dangling bonds) we found Δ=-1.8 and -1.9 eV respectively with respect to the $N\text{-}Si_3$ peak. In fact, the overall dielectric environments at the nitrided Si(001) surface and the nitrided $Si(001)\text{-}SiO_2$ interface are not too different (ε_∞ = 2.1 for SiO_2 with respect to ε_∞ = 1 for vacuum). This explains why the N 1s core-level shifts in both systems can be interpreted in terms of a common scheme which primarily depends on the atoms in the nearest neighbor shell.

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Integrated processing of ALCVD™ high k gate stacks with RTP based interface and electrode layer formation

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One of the historically most challenging undertakings in the wafer processing industry is the replacement of the SiO_2 based gate dielectric technology, which served the industry for more than 30 years, by a new generation of materials. Leakage current improvement over SiO_2 is the driving force for this change and for that, the successful integration of materials with a higher permittivity (k value) than SiO_2, is a pre-requisite. This paper reviews the capabilities of a multi-chamber cluster tool which includes processing modules specifically developed to address the integration issues that emerge with the use of high k dielectrics.

Process control in the ultra thin (0.5-5.0nm) thickness regime is of extreme importance and results can be expected to be influenced by wafer surface properties. As the removal of a chemical cleaning oxide or an accidental native oxide on the silicon channel area is required to reach a low enough electrical layer thickness, this step is preferably done in the cluster tool itself rather than in a separate processing system. In the former case wafer transport takes place under high purity, vacuum conditions rather than fluctuating environmental conditions.

An HF/Acetic acid vapor based chemistry is described that removes both accidental organic contamination and any surface oxide on Si, at room temperature. The process is executed in a separate module under reduced pressure with all metallic, gas exposed surface areas of the inner reactor chamber coated by a polymer in order to avoid metal contamination of the wafer. Results are included that demonstrate the successful use of this process step prior to dielectric layer formation.

Among the most stringent requirements for a successful replacement of the SiO_2 dielectric is a sufficiently reduced leakage current but with little to no drive current reduction. This means that without an "SiO_2 like" interfacial layer between the silicon channel area and the high k dielectric film, chances are that mobility will be degraded due to less "ideal SiO_2" bond structures at the interface leading to defect induced charge trapping at the interface. For that purpose, the cluster tool mentioned has a specific "Interface Preparation" module with extremely flexible process parameters that allows the formation of ultra thin layers of SiO_2, Si_3N_4 and mixtures of thereof. A variety of chemistries are used and examples are given for pure thermal oxidation and nitridation processes. The purpose of the addition of nitrogen in the interface film is to promote chemical stability and reduce diffusion of polysilicon gate electrode dopants into the channel area.

When the above process steps are completed, the high k dielectric layer is formed by a novel ALCVD™ process. The construction of the corresponding reactor is such that conventional CVD is suppressed well below the 0.1% regime, resulting in extremely

stoichiometric films with very low levels of precursor gas residues and consequently, low leakage currents. High k oxides that are routinely deposited include Al_2O_3, ZrO_2 and HfO_2. Gas control is performed by a patented technique using inert gas as a high-speed pulse "valve". Because of its high ALCVD content, also nano-laminate structures of ultra thin layer stacks can be formed with very abrupt interfaces. As will be reviewed, this feature is of extreme importance to stabilize the amorphous phase of the as-deposited layers without a too large of a penalty in k value. All of the above allowed the formation of films with electrical thickness values well below 1.0nm and record low leakage currents.

The fourth module on the cluster has basically the same reactor structure as the mentioned "Interface Preparation" module but the hardware is designed to support (conventional) CVD of in-situ, or undoped Si or SiGe layers which act as gate electrode. For that reason some basic properties of these films are discussed next to some specific issues that relate with the compatibility of Si materials and the corresponding CVD process, with high k oxide substrates. To cope with Si depletion effects that inherently limit the electrical thickness scaling of high k dielectrics, this CVD module can be replaced by a second ALCVD™ module that can deposit TiN or WN as " midgap" electrode materials. Work is in progress to develop also work function matching metals for n type and p type transistors, like TaN and Ru, respectively

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Electronic Structure Study of Al_2O_3 in the Cluster Approach: What does it take?

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Al_2O_3 has emerged as a potentially attractive candidate to supplant amorphous *a*-SiO_2 in metal-oxide-semiconductor (MOS) technology due to its large band gap, good thermal stability in direct contact with Si, and relatively low density of defects. Unlike *a*-SiO_2, however, little is known about the microscopic structure of the bulk oxide, presence and effects of point defects on electronic and electrical characteristics, and the chemistry and physics of the oxide-Si interface in the case of Al_2O_3. First-principles quantum chemical studies of electronic structure and properties of SiO_2 in the "cluster approach" have provided detailed understanding of its microscopic features, particularly those related to the chemical bonds and point defects. Therefore, one anticipates that similar studies in the case of Al_2O_3 would provide valuable information related to its microscopic features. With such a goal, we have begun a systematic *ab initio* electronic structure study on Al_2O_3 in cluster approach. Calculations have been performed on Al_2O_3 clusters of increasing dimension and complexity with the use of *ab initio* Hartree-Fock (HF) method and extended one-electron basis functions.

Unlike a-SiO_2, the structure optimizations of aluminum oxide clusters have proven to be very challenging. The geometry of one of the clusters used for structure optimization is shown in Fig. 1. The Al atoms in this cluster are alternately coordinated to 4 and 6 oxygen atoms. This particular coordination pattern was taken from the structure of the γ-Al_2O_3. The non-bridging oxygen atoms are capped with H atoms to satisfy valency requirements. No stable structure that retains this coordination pattern is found upon optimization of the initial structure. Instead, unusual bond formation and bond-breaking events follow the optimization process, leading to a structure like that shown in Fig. 2. Other calculations involving a $Al(OH)_4$ cluster and a simple Al-substituted SiO_2 cluster also did not lead to stable structures. These observations raise an important question: Are cluster-approach calculations inappropriate for electronic structure investigations of ionic oxides, such as Al_2O_3? Unfortunately, the results of our initial calculations are not very encouraging. We are examining the effects of such factors in the calculations as the quality of the basis set, electron correlation, and the size and morphology of the cluster. Detailed results of our theoretical modeling effort will be presented at the conference.

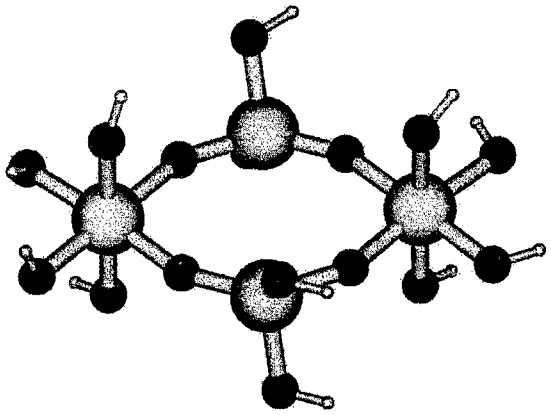

Figure 1. Starting configuration for an Al_2O_3 model cluster. The Al atoms in the ring are alternately coordinated to 4 and 6 oxygen atoms. The valence of the outer oxygen atoms is saturated with H atoms.

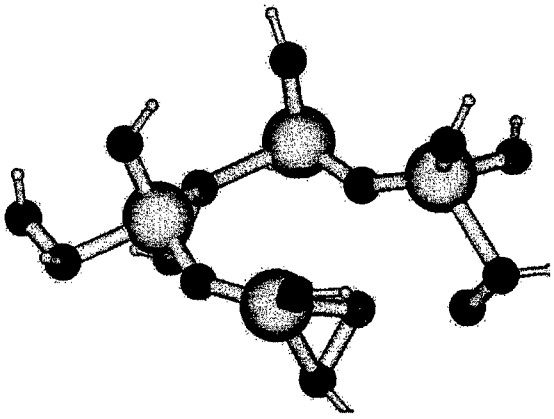

Figure 2. One of the energy-minimized configurations resulting from the optimization of the structure shown in Fig. 1.

Abstracts (Posters)

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Growth of sub-1 nm EOT gate quality ZrO_2 and HfO_2 films by MOCVD using TDEAZ and TDEAH precursors

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The continued scaling of MOSFET devices is likely to require the replacement of the SiO_xN_y gate dielectric with a high-k film at some point in the sub-100 nm technology nodes for specific high performance and low-power applications. HfO_2 and ZrO_2 and their alloys with SiO_2 are currently among the leading candidates for high-k gate dielectric application. Gate quality ZrO_2 films were deposited by a metallorganic chemical vapor deposition (MOCVD) process in a high-volume production capable tool at International SEMATECH using tetrakis-diethyl amido zirconium (TDEAZ) as a precursor. TDEAZ is a stable liquid precursor that can be readily delivered by currently available standard liquid delivery systems from various tool suppliers. Many amido type high-k precursors offer many advantages such as high vapor pressure and resistance to hydrolysis compared to other liquid and solid precursors like alkyl oxides, halides and diketonates.

ZrO_2 films were deposited on 200 mm (100) oriented silicon wafers prepared with an SC1/SC2 cleaning process over a temperature range of 235°C to 485°C and extensively characterized using a variety of analytical techniques. The carbon content in the films, as measured by Auger electron spectroscopy, was found to decrease from 5% for films deposited at 310 °C to about 2% for films deposited at 485 °C. The film growth rate was found to be reaction rate limited below 300 °C and mass transport limited at higher temperatures. In the mass transport limited regime, the growth rate was found to decrease linearly as the temperature was increased from 300 °C to 485 °C. Extensive cross-section TEM analysis showed that the ZrO_2 film deposited at 485 °C is almost entirely polycrystalline and the degree of the crystallinity decreases with decreasing film deposition temperature. The ZrO_2 films deposited at 310°C were found to be almost entirely amorphous with less than 5% crystallinity. The micro-structure of the film was also observed to be strongly dependent on the film thickness. Thinner films (< 8 nm) exhibited a lower degree of crystallinity and surface micro-roughness compared to relatively thicker films grown at the same temperature. Thicker films (> 20 nm) deposited at ≥ 400°C were found to have columnar grains spanning the entire thickness of the films. The pre-gate clean used before the high-k film deposition strongly influences the growth of the high-k film in the initial stages as well as the final interface between the high-k film and the Si substrate. Various interfacial annealing treatments on the Si substrate before the high-k deposition were evaluated and it was found that the control of the interface is the most critical step in achieving sub-1 nm equivalent oxide thickness (EOT), as well as achieving low gate leakage current density (J_g) and flat-band voltage (V_{fb}).

MIS capacitors were fabricated using a variety of interfacial substrate annealing treatments, ZrO_2 and HfO_2 film deposition conditions, as well as post-deposition annealing treatments. The high-k gate dielectric films were capped with PVD deposited TiN and TaN as gate electrodes. Detailed capacitance-voltage (C-V) and leakage current characterization (I-V) were performed using 3 different capacitor sizes as well as multiple a-c frequencies. It was observed that the post-deposition annealing strongly affected EOT, J_g and V_{fb} for high-k films

deposited at temperatures ≤ 310°C. On the other hand, the interfacial annealing step was found to be the most critical step for films deposited at temperatures > 400°C. The role of each of the key processing steps in achieving sub-1 nm EOT films with low leakage and related electrical results will be presented.

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Analysis and fabrication of MOS capacitors with PECVD SiOxNy insulating layer, deposited by PECVD

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Increasing scale integration requires the search for insulating layers with higher refractive index and obtained at low temperatures (<400^{0}C). Since the gate dielectric thickness and the channel length in MOS transistors continue to decrease, high temperature processing cycles (~1000 ^{0}C) cause Boron penetration from the P+ polysilicon gate, through the very thin SiO_2 insulating layer, as well as lateral diffusion of the source and drain regions. [1]. Silicon dioxide is also presenting other limitations as poor stability of the Si/SiO_2 interface, resulting from the high stress/ strain associated with volume expansion of SiO_2, which degrades the device life time [1].

In order to overcome these limitations research is being oriented to the effect of nitrogen incorporation in the dielectric layer [1,2,3]. Nitrogen will act as a very effective barrier to boron diffusion [1,4,5] and decreases the intrinsic stress improving the $Si/SiOxN_y$ interface stability such as the charge- to-breakdown (Q_{bd}) thus increasig device life time [1]. Also the dielectric constant of the material increases permitting the utilization of thicker insulating layers for the same capacitance than thin oxides [4].

In previous works we demonstrated the possibility of obtaining stoichiometric SiO_2 utilizing the PECVD technique, exhibiting structural properties and refractive index very similar to thermally grown material, and thus very promising for applications as gate insulator in MOS devices [5]

In this work we fabricate MOS capacitors utilizing as insulating layer PECVD $SiOxN_y$ with variable Nitrogen concentration in order to analyze the effect of nitrogen concentration on the electrical characteristics of the devices. Also the structural and physical properties of the films are characterized by ellipsometry, FTIR spectroscopy and RBS.

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Electrical properties of metal-oxide-semiconductor capacitors with ultra-thin silicon oxide films

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This research addresses the C-V and I-V characteristics of n^+/p and n^+/n MOSCAPs with scaled-oxide thickness values (i.e., 1.5 to 2.4 nm in steps of 0.3 nm). Model-based analyses of statistically sampled C-V data sets return the following metrics: effective oxide thickness; flatband voltage (or effective interface charge density); doping density of the polysilicon-gate electrode and the silicon substrate; metal-semiconductor work function difference; and oxide fixed charge. The results of these analyses demonstrate that the extracted values of the effective oxide thickness (t_{EOT}) scale with expectation (i.e., Δt_{EOT} is ~ 0.8 nm). Hence, it is concluded that the trends in the remaining electrical metrics are representative of MOSCAPs with near-atomically scaled ultra-thin silicon oxide films. Model-based analyses of statistically sampled I-V data sets return the area dependence of the current at a given bias voltage and hence, from a linear least-squares analysis, the current density (J) for both gate-electrode injection (i.e., n^+/p MOSCAP) and substrate injection (i.e., n^+/n MOSCAPs). The results of these analyses demonstrate that both gate-electrode and substrate injection generate nearly the same current density relative to flatband voltage (i.e., reciprocity holds for these devices). In addition, it is possible to assess the relative accuracy of the effective oxide thickness (t_{EOT}) values from the relative change in current density (J) and a theoretical rule-of-thumb that says a change in t_{EOT} of 0.2 nm will result in a fractional change of one decade in J. The differences in oxide thickness for both the n^+/p and n^+/n wafers are both ~ 0.8 nm and the fractional change in current density is about four decades. Hence, it is concluded that the relative accuracy of the effective oxide thickness values is quite high. Since a post-metallization-anneal (PMA) was not included in the original process sequence, the second phase of this research is addressing the impact of a PMA on the no PMA electrical metrics for the same device wafers.

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Proton radiation hardening of ultra-thin silicon oxynitride gate nMOSFETs formed by low-energy nitrogen implantation into silicon with additional conventional or rapid thermal oxidation.

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The effects of proton-induced damages on the performance of metal/silicon oxide/silicon devices have been investigated [1]. The proton bombardment ionization into silicon oxide creates defects, such as electron-hole pairs. Consequently, hole and electron transport and/or trapping processes in oxide can occur, in the case low oxide radiation hardening, reducing the device performance. Silicon oxynitrides, other than oxides, have been employed to produce radiation hardened MOS devices [2]. The effect of nitrogen, near the insulator/silicon interface, on charge trapping improves the oxynitride radiation hardening. In this work, silicon oxynitride (SiO_xN_y) insulators have been obtained by low-energy nitrogen ion implantation (N_2^+ ion beam energy of 5keV and doses of 10^{14} or 10^{15} cm^{-2}) into Si substrates prior to conventional or rapid thermal oxidation. Theses films have been used as gate insulators in enhancement nMOSFETs and MOS capacitors [3]. MOS capacitors were used to obtain capacitance-voltage(C-V) measurements. A relative dielectric constant of 3.9 was adopted to extract the film thickness from C-V curves, resulting in values between 5 nm and 12nm. nMOSFETs were bombarded with H^+ ion beams (energy of 170 keV and fluences of 0, 10^{12}, 10^{13} and 10^{14} protons/cm^2) to investigate radiation hardening. nMOSFET electrical characteristics, such as threshold voltages(V_T), transconductances(Gm) and sub-threshold slope(S), were extracted before and after proton radiation. For high dose bombardment, Gm is reduced, V_T and S are increased. From the study, the following main considerations are obtained:

- nitridation by N_2^+ ion implantation leads to an inhibition effect on the thermal oxidation of Si, in the rapid and in conventional processing. This inhibition effect is increased for higher implanted nitrogen fluences.
- nitridation by N_2^+ ion implantation prior to conventional or rapid thermal oxidation improves the device performance in terms of threshold voltage shift, transconductance and sub-threshold slope.
- nitridation by N_2^+ ion implantation prior to conventional thermal oxidation improves the quality of the dielectric film in terms of radiation hardening.
- nitridation by N_2^+ ion implantation prior to rapid thermal oxidation improves the quality of the dielectric film in terms of radiation hardening when an appropriate nitrogen fluence of $10^{14}/cm^2$ is used.

In this way, nMOSFETs with high quality ultra-thin oxynitride gate have been fabricated. These oxynitride gate devices can be used for radiation hardening applications. Up to proton fluences of $10^{12}/cm^2$ are endured by the films.

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Monolayer incorporation of nitrogen during remote plasma oxidation of Si in plasma oxidation of Si in N_2O and N_2O+N_2.

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Ultra-thin silicon oxynitride films (SiO_xN_y) have attracted considerable attention to sub-micron MOS gate insulators due to their potentially improved properties in comparison with other dielectric layer such as SiO_2. Some of its characteristics include low defect density, high dielectric breakdown fields, low impurity diffusion, high radiation hardness and reduced tunneling current. The improved dielectric reliability is mainly due to the pile up of the incorporated nitrogen in the vicinity of the SiO_2/Si interface. The Si-N bonds replace the strained Si-O bonds at the SiO_2/Si interface, decreasing the interface strain.[1-4]

Silicon oxynitride films can be prepared by a number of techniques. Conventional furnace oxidation in N_2O and rapid thermal oxidation in N_2O and NO have been used for the N atom incorporation at SiO_2/Si interfaces. [2, 5-7] These processes involves temperatures higher than 1000°C. As alternative for N incorporation at low temperatures, one has the remote plasma oxidation (RPO) process. Its lower temperature capability is due to addition of plasma energy to the environment in the form of a glow discharge.

This paper focuses on N incorporation at SiO_2/Si interfaces by the low temperature RPO process (300°C) using N_2O and N_2O+N_2 ionized in microwave fields (2.45GHz and 600W) as source for oxygen and nitrogen atoms performed by a home-made RPO plasma system. This system allows oxidation/nidridation/oxynitridation as well as deposition processes, depending of the gases involved in the process. Also, one can perform rapid thermal annealing *in situ* avoiding ambient contamination between the processes. This can be performed by a halogen lamps array that maintain a substrate temperature up to 300°C.

X-ray photoelectron spectrometry (XPS) and secondary ion mass spectrometry (SIMS) analysis confirmed the low N incorporation in the Si/SiO_2 interfaces. The ellipsometric, etching rates measurements and transmission electron microscopy (TEM) analysis presented thickness up to 5.5nm.

A model has been proposed to explain the variation of the composition of the Si/SiO_2 interfaces as a function of ambient plasma oxidation. TEM revealed a thinner oxyninitride films grown in N_2O and N_2O+N_2 plasma with higher N concentration, confirming the self-limiting growth of silicon oxide due to the blocking of oxidant diffusion by interfacial nitrogen. Also, we can see a low roughness profile indicating a high quality interfaces formed by RPO process.

Electrical properties indicated that the oxide films formed have presented high quality, low N incorporation given by dieletrics constants, very low effective charge density of $1.7x10^{10}/cm^2$ up to $2.3x10^{11}/cm^2$ with a 10 minutes sintering time and high breakdown E-fields of 15.4 MV/cm to 18.3MV/cm. These high qualities allow that these films, formed with a reduced thermal budget, can be used as gate dielectric in MOS devices on Si substrates.

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Electrical characteristics of aluminum oxynitride gate pMOSFET formed by sputtering DC deposition in nitrogen ambient with additional rapid thermal oxidation and annealing.

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Aluminum oxynitride (AlO_xN_y) became a promising material for silicon and III-V compound semiconductor devices due to its thermal stability and high dielectric constant [1-2]. Aluminum oxynitride (AlO_xN_y) insulators have been obtained by sputtering DC deposition, using different deposition times of 5s, 20s, 30s and 90s, in nitrogen ambient with additional rapid thermal oxidation and annealing at temperature of 960^{0}C for 40s. Theses films have been used as gate insulators in enhancement pMOSFETs. These devices and MOS capacitors, with Al electrodes and final sintering time at 450 ^{0}C for 10 min in N_2+H_2O(v), were fabricated. MOS capacitors were used to obtain capacitance-voltage (C-V) measurements. A relative dielectric constant of 9 was adopted [1] to extract the film thickness from C-V curves under strong accumulation condition, resulting in values between 14 nm and 38 nm, and the effective charge densities of about 10^{11} cm^{-2}. pMOSFET electrical characteristics, such as threshold voltages between –1.1V and –1.5V, transconductances between 50 μS and 144 μS, sub-threshold swings between -65 mV/dec and -160 mV/dec, were obtained. These results indicate that the obtained AlO_xN_y films are suitable gate insulators for metal-oxide-semiconductor (MOS) devices.

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Interfacial diffusion studies of Hf and Zr into Si from thermally annealed Hf and Zr silicates

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$HfSi_xO_y$ and $ZrSi_xO_y$) are some of the promising high-κ gate dielectric candidates which are expected to meet the predictions of the SIA technology roadmap, especially the need of less than 2.0 nm SiO_2 gate dielectric for sub-0.13 μm scaled silicon CMOS [I]. Desirable properties for new gate dielectrics include; higher permittivity (κ), than SiO_2 (κ = 3.9), low leakage current (<1 A/cm^2 @ 1V) and thermodynamic stability at the interface with silicon. Considering these requirements, Hf silicate and Zr silicate have been proposed as suitable candidates for advanced gate dielectric applications [II, III, IV]. However, the stability of the gate dielectric/silicon interface following dopant activation annealing remains one of the most important issues to be solved. Any Zr or Hf metal diffusion into the channel is critical because impurity diffusion from the gate dielectric into the channel region would likely result in deleterious effects on carrier mobility.

Diffusion studies of Hf and Zr from high-κ gate dielectric thin films (4-5 nm) candidates $HfSi_xO_y$ and $ZrSi_xO_y$ into Si were undertaken. Two similar sets of gate dielectric structures were subjected either to rapid thermal processing (RTP) or standard furnace annealing in N_2 atmosphere for comparison purposes. The annealed structures were then chemically etched prior to depth profiling using both ToF-SIMS and a combination of Heavy Ion Rutherford Backscattering Spectrometry (HI-RBS)/UV-ozone oxidation/etching cycles. The chemical make up of both the as-deposited and annealed films were studied using monochromatic X-ray Photoelectron Spectroscopy (XPS), High resolution TEM was used to monitor any structural changes or growth of an interfacial film initially present (most likely SiO_2) in the as-deposited gate dielectric/Si structures. Film deposition, chemical etching and characterization issues are discussed. No significant Hf diffusion into Si was observed for both RTP and furnace-annealed films. The Zr diffusion into Si was more pronounced when compared to Hf. Implications for high-κ gate dielectric applications are also discussed.

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Biomimetic processing of oxide thin films for gate dielectrics

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Living creatures have developed techniques to synthesize inorganic materials with various compositions at specific sites with required size and shape to meet their own purposes. This clever process which is called biomineralization is a soft solution process in itself, and it is based principally on the interactions at organic/inorganic interfaces which are controlled in the biological environment at ambient temperatures consuming only a small amount of energy. We should learn from this process to develop novel environmentally benign processing methods for the future materials manufacture.

Information technology and microelectronics/photonics of the 21st century would require techniques to fabricate functional materials and devices exquisitely with required size and shape on a small length scale, and this process seems to be similar to what living creatures are doing. This analogy motivated us to develop new methodology to construct electronic devices by biomimetic processing.

This paper reviews the state-of-the-art of biomimetic fabrication of oxide thin films for gate dielectrics, which is currently investigated in our laboratory. Examples of micropatterning of dielectric thin films of TiO_2, Ta_2O_5, etc. achieved through the deposition from liquid solutions onto self-assembled monomolecular layers (SAM) will be presented, and I-V and C-V characteristics of MOS structures associated with the processing and resultant microstructure will be discussed.

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Electrical characterization of sub-2 nm EOT gate dielectrics on silicon

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As the semiconductor industry strives for smaller and faster devices with lower operating voltages, many issues need to be addressed in order to reach targeted objectives. One critical issue is the scaling of device dimensions as defined by the International Technology Roadmap for Semiconductors (ITRS) Roadmap. As MOSFET dimensions are scaled (i.e., length, width, extension junction depth), the dielectric film thickness must also be reduced. Indeed, the gate dielectric thickness is the smallest fabricated dimension in MIS transistors today. Characterization of the MIS capacitor is accordingly a most crucial element in the development of future MIS structures and devices that are necessary to meet the ITRS guideline trends.

The MIS capacitor is used extensively in research as a process control structure that addresses the need for characterization of ultra-thin oxynitides and alternative high-k gate dielectrics. Electrical testing of these MIS structures through Capacitance-Voltage (C-V), Current-Voltage (I-V), and reliability measurements provide valuable ITRS parameter information in an expeditious manner.

Although electrical characterization is an ideal way to extract valuable parameters, precautions must be taken in the actual testing and subsequent data analysis. Characterization equipment must have low stray parasitics and a correction factor for these stray parasitics is often necessary. The parasitic correction factor minimizes errors in parameter extraction models that do not account for stray parasitics in the model derivation. In the ultra-thin oxynitrides and high-k gate dielectric regime, gate leakage is a major concern when extracting parameters from C-V measurements. Additionally, dielectric breakdown can be hard to determine in the ultra-thin regime due to soft breakdown.

There are several promising techniques that can be used to address the concerns presented above. Two techniques that aid in minimizing the effects of gate leakage are: dual frequency, 3-circuit element correction [1] and a fully distributed transmission line along the gate length [2]. For soft-breakdown detection, a noise-based trigger detection algorithm appears to be an excellent candidate [3]. Applicability of reliability techniques such as SILC, CVS, etc. that have been used for ultra-thin SiO_2 needs to be established for these alternative dielectrics to assure development of gate dielectrics that will be required for the 100 nm and smaller technology generations. Demonstration of these techniques with representative evaluations of silicon oxynitride as well as high-k films will be presented to provide insight into how C-V, I-V, and reliability characterization can be used in the evaluation of alternative high-k gate dielectrics.

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Influence of the oxynitridation parameters on the refractive index and on the thickness uniformity of MOS gate dielectrics grown by RTN

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The search for MOS devices with reduced dimensions requires ultrathin gate dielectrics whose main characteristics should be: resistance to radiation and hot carriers generation, ability of stopping impurities and dopants from the bulk, high breakdown dielectric fields, low density of interface states and low density of bulk trapped charges [1,2,4]. In this work, silicon oxynitrides were manufactured by rapid thermal processing (RTP), using O_2 and N_2O gases at temperatures above 1050°C.

Silicon wafers, 3 inches in diameter, with <100> crystalline orientation, (381± 50) μm thick, n-type and resistivity in the range of 1 to 10 Ωcm were used. All wafers underwent complete chemical cleaning (piranha + RCA + HF) [3]. After cleaning, they were processed by rapid thermal oxidation, rapid thermal nitridation and annealing in nitrogen for temperatures above 1050 °C, and processing times varying between 30 and 500s by using a RTP oven, model 410T from Steag-AG.

A 200-point-mapping of the thickness and standard deviation for the oxynitride films was carried out by ellipsometry. In addition, the thickness difference between the center and the edge of each wafer was also obtained. The results showed that the SiO_2 films were thicker at the center than at the edge [5] and the standard deviation was 11.2%. On the other hand, SiO_xN_y films resulted thicker at the edges than at the center, and the standard deviation resulted as low as 5.3%. The lower thickness for the SiO_xN_y films at the center of the wafer was attributed to the presence of a thicker rich layer of nitrogen due to the slowly higher temperature there during the RTN step compared to the edge.

SiO_2 and SiO_xN_y films underwent a wet etching to obtain square structures in order to measure their heights (thickness) by AFM. After that, such measured values were used in an ellipsometric system (AUTOEL II from Rudolph, Inc.) in order to obtain their refractive index, whose values were used to calculate the electrical permissivity, the nitrogen concentration and the films stoichiometries for T≥1050 °C.

All the results were confirmed with X-ray Photoelectron Spectroscopy (XPS) analysis, which presented binding energies of 397.6 eV (Si-N bonds) and 400.9 eV (Si-N-O bonds).

The Si oxidation performed in N_2O ambient, produces gate dielectrics with better uniformity for the thickness and higher refractive index, due to the presence of nitrogen after decomposition of N_2O gas, as measured by XPS analysis. In this case, the Si oxidation rate is reduced at the center of wafer, where the temperature is slowly higher compared to its edge.

Table 1: Obtained values of refractive index, electrical permissivity, nitrogen concentration and stoichiometry of the oxynitride films:

Process time (s)	30	500
Refractive Index	1.48	1.53
Permissivity	4.02	4.28
N Concentration (%)	12	16
Stoichiometry	$Si_{1,1}$ $O_{1,93}$ $N_{0,14}$	$Si_{1,2}$ $O_{1,8}$ $N_{0,40}$

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Challenges of electronic structure calculations on Zr and Hf oxides

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Ab initio Hartree-Fock cluster methods have proven very useful in understanding the microstructural features of Si-SiO_2 systems. In particular, these methods have provided a detailed understanding of the physics and chemistry of point defects at the Si-SiO_2 interface and in the oxide. In view of the technological importance of alternate dielectric systems to supplant SiO_2 in MOS technology. We have recently begun a program to systematically investigate the microscopic structure and electronic properties of Zr and Hf oxides using the same *ab initio* cluster approach.

To this end, Hartree-Fock calculations have been undertaken on candidate structures using a relativistic effective core potential (ECP) basis set. For our initial studies, we have focused on determining the local environment surrounding a single Zr or Hf atom and have constructed clusters in which the Zr or Hf atoms are surrounded by 7 oxygen atoms arranged as they are believed to be in the monoclinic forms of the oxides. The valency of the oxygens is saturated with H atoms. *f* polarization functions have been added to Zr and Hf, *d* polarization functions have been added to the O atoms and *p* polarization functions have been added to the H atoms. The starting point for our model calculations is to obtain the optimal arrangement of the O atoms around the central nucleus by energy optimization. A typical starting configuration is shown in Figure 1.

Unlike the Si-SiO_2 systems, the structural optimization of Zr and Hf oxides have proven to be very challenging. In both the Hf and Zr systems, we observe that the optimized structures do not retain their original monoclinic symmetry and coordination. The microscopic features of the optimized structure depend upon the basis set employed in the calculation, but typically involve the ejection of 1 or more O atoms from the coordination sphere. There may be several reasons for observed behavior: (1) choice of the dimension of the atomic cluster employed, (2) choice of basis set , (3) choice of terminating atoms, and (4) chemical effects in ionic oxide clusters. Additional studies directed at identifying these effects are under way. Details of the study and our findings will be presented at the conference.

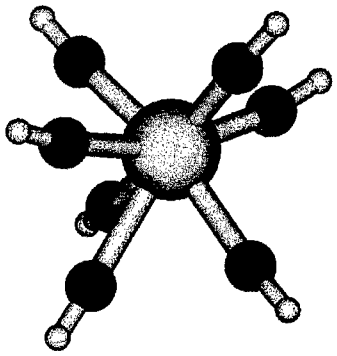

Figure 1. Starting guess for configuration of atoms around a single Hf nucleus.

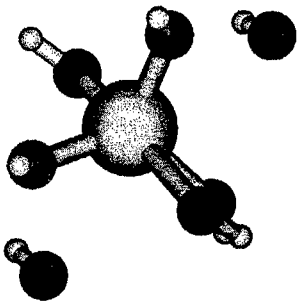

Figure 2. Result of structure optimization of Hf oxide shown above using an ECP basis set with f polarization functions on the Hf atom, d polarization functions on the O atoms, and p polarization functions on the H atoms. Two of the O atoms have moved to positions over 3Å from the Hf atom, 4 of the O atoms remain at approximately 2 Å from the Hf atom, and the remaining O atom is located at approximately 2.6 Å away.

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Characterization of ultra-thin dielectric layers

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The material or materials which eventually replace SiO_2 as gate dielectrics will be chemically more complex than SiO_2. As with SiO_2, film thickness and uniformity measurements will remain important but, in addition, the determination of the chemical composition of the materials will become more important. The uniformity of composition and the interactions taking place at the interface between the new dielectric and the silicon or silicon dioxide substrate will need to be determined.

As the films become more complex, traditional methods, such as ellipsometry, will be unable to provide unambiguous measurements. SIMS can provide depth profiles showing the elements present but there is always the danger that the artefacts associated with SIMS will provide misleading results or the sputtering process, on which SIMS depends, will alter the chemical states of the materials in the layer.

This paper will show how X-ray Photoelectron Spectroscopy (XPS) and Angle Resolved XPS (ARXPS) can be used to characterise these advanced, ultra-thin films of dielectric materials. It is well known that XPS provides chemical state information from the near surface region (10 to 15 nm, depending upon the material). Quantification of XPS data is also possible and widely practised. With ARXPS, measuring the XPS spectrum at a range of electron escape angles can control the information depth. Photoelectrons emerging from the surface at near grazing emission angles will provide information from the near surface region while those emerging at near normal emission angles provide information about both the surface and rather deeper regions of the material. This phenomenon can be used to determine the composition and thickness of the film.

Traditionally, ARXPS measurements have been achieved by making an analysis, tilting the sample, repeating the analysis and continuing until the required range of angles had been covered. This method has a number of disadvantages. The technique was slow and can not be applied to full wafers. In this paper we will show how all of the angular information can be collected simultaneously without the need to tilt the sample. This development makes the technique available for characterisation of ultra-thin dielectric layers on complete wafers. This provides a non-destructive method for obtaining information about thickness, uniformity, composition, chemical states and interface chemistry.

Examples will be given to show how the technique has been applied to a range of dielectric materials on a silicon substrate.

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Fixed charge and interface traps at heterovalent interfaces between Si(100) and alternative high-k gate dielectrics

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Interfaces between Si(100) and the high-k gate dielectric candidates, Al_2O_3, Ta_2O_5, and HfO_2, and their alloys have been prepared by remote plasma enhanced deposition at 300°C onto H-terminated Si(100) substrates using metal-organic and nitrato metal atom sources. Interfaces were compared with those formed by a two step process: i) remote plasma-assisted oxidation at 300°C to form ~0.5-0.6 nm of Si oxide, followed by ii) plasma deposition of the same high-k dielectrics. Interfacial bonding at initial stages of film deposition was monitored by on-line Auger electron spectroscopy, AES. Comparisons between AES spectra as a function of metal oxide deposition time corresponding to >1.0 nm of Al_2O_3, Ta_2O_5 and/or HfO_2 indicated ~0.5-0.6 nm of silicon oxide formed during deposition onto the HF-last Si substrates. This thickness of the interfacial silicon oxide layer was confirmed for Al_2O_3 depositions by resonant nuclear reaction analysis, and by electrical measurements of flat band voltage shifts for capacitors with Al_2O_3 layers of different physical thickness.

This paper addresses two aspects of high-k/Si interfaces that impact significantly on the electrical performance and reliability in advanced CMOS devices. First, the high-k dielectrics of this paper are considerably more ionic than SiO_2, and as a result their interfaces with Si are inherently heterovalent in the sense that a balance between nuclear and bond charge is not possible without creation of bonding defects. Paralleling what is known for heterovalent interfaces between different semiconductors, e.g., Ge and GaAs, this results charged interfacial defects [1]. Additionally, there is an interfacial transition region comprised of Si-O bonds that contributes adversely to the capacitance.

Analysis of capacitance- and current-voltage, C-V and J-V, data on test capacitor with n-type and p-type substrates indicates high levels of fixed charge, and interfacial electron traps. The temperature and thickness dependencies of C-V and J-V traces compared with SiO_2 devices provides an unambiguous way to distinguish between fixed charge and traps. Fixed negative charge in the mid 10^{12} cm^{-2} range is at the Al_2O_3 interface after a post metallization anneal in forming gas, and interfacial trap densities are also in the 10^{12} cm^{-2} range. Trapping is significantly increased by addition of alloy concentrations of Ta_2O_5. Analysis of J-V and C-V data give activation energies for trapping and trap release in agreement with conduction band offset energies derived from XPS studies of Miyazki [2]. The activation for electron injection into Ta traps is 0.30±0.05 eV, consistent with the energy of empty Ta-atom d-states relative to the Si conduction band. The activation energy for trap release is 1.5±0.1 eV, in agreement with the energy difference between Ta-atom d-states and the Al_2O_3 conduction band [2].

Finally, the interfacial Si oxide layers films formed during film deposition contribute ~0.35 nm to the effective oxide thickness. This reduces the thickness of the high-k dielectric for a targeted capacitance by approximately $0.09k_d$ in nm. This decrease in thickness can increase direct tunneling at ~ 1 V by a factor ranging from 10^2 to 10^4.

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Selection and Growth of Alternative High-*K* Materials for Gate Oxides

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The need for an alternative higher-*K* gate oxide for silicon MOSFETs has led us to compile a comprehensive list of multicomponent oxides that are likely to be thermodynamically stable in contact with silicon. Unfortunately, limited experimental data for the dielectric constant and bandgap of many of these compounds exists, precluding the clear identification of the most suitable material for implementation in MOSFETs. Using the floating zone and Czochralski crystal growth methods we have grown single crystals of many of these compounds and measured their dielectric constants and bandgaps. The result is a nearly comprehensive list of Si-compatible binary and ternary oxides, 14 of which have a dielectric constant over 20 and at least 7 of which have a bandgap over 5 eV. Based on these experimental results we have selected $LaAlO_3$ and $LaAlO_3$-related materials (e.g., La_2O_3, La_2SiO_5) for investigation as alternative gate dielectrics for silicon MOSFET's. Using an oxide molecular beam epitaxy system, we have grown epitaxial thin films of $LaAlO_3$ on a thin epitaxial buffer layer of SrO on Si (100) substrates. Initial electrical characterization of these films, however, has indicated that this SrO buffer layer degrades at the high temperatures required for the growth of these materials. The growth of epitaxial $LaAlO_3$ directly on silicon is extremely difficult due to the high oxygen pressures required for the oxidation of La and the presence of a low temperature eutectic between Al and Si. Therefore, our initial investigation has focused on polycrystalline/amorphous $LaAlO_3$ films grown directly on silicon. High-resolution TEM images of these films show no interfacial reaction layer. Electrical measurements reveal that these films have an average dielectric constant of 18 and a capacitive equivalent thicknesses (CET) of 11Å. In addition, polycrystalline/amorphous La_2O_3/La_2SiO_5 films have been investigated and have CET values below 10Å and leakage below $1A/cm^2$ at 1V. Detailed structural (high-resolution transmission electron microscopy, reflection high-energy electron diffraction, and x-ray diffraction) and electrical data on all of these films will be presented in addition to the data on which our comprehensive selection process was based.

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S. Karna's and A. C. Pineda's abstracts were withdrawn. There is one more abstract:

STRUCTURAL ORDER AND CLUSTERING IN ANNEALED a-SiC and a-SiC:H

Cesar R. S. da Silva, J. F. Justo, and A. Fazzio

We carried out a theoretical investigation on the structural properties of annealed a-SiC and a-SiC:H. The calculations were performed using free volume Monte Carlo method combined with interatomic potentials.Our prototype nanoparticle contained as much as 85000 atoms which allowed for a superior statistical sampling of the material. Our results show that C atoms segregate, forming small clusters embedded in an extensive Si network. Si atoms are rather forming large networks with few small clusters. Unprecedented detailed ring statistics analysis show that C clusters are ramified, and that H introduction increases the incidence of micro-voids in the structure. Additionally, H incorporation slightly reduces the chemical order in the material, and, in a larger extent, reduces the mid-range structural order. Hydrogen also relaxes bonding stress around atoms in the network. Our results are consistent with the available experimental data.

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